USER´S MANUAL

4MEG VIDEO Model 12
Revision 4.2

6 November 2000

For use with:
4MEG VIDEO Model 12 Rev. 4.2

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1. Installation and Features

This manual refers to both the 4MEG VIDEO Model 12 Revision 4.0 and 4.1. The term 4MEG VIDEO or Model 12 will be used to refer to the 4MEG VIDEO Model 12.

The "PC memory base address" refers to the 64K address segment that is used by the 4MEG VIDEO Model 12. The default is 0xD0000. The prefix "0x" denotes a hexadecimal number. Reference is made to EPIX' 4MIP software.

1.A Unpacking and Static Warning

The 4MEG VIDEO Model 12 is packed in a static dissipative bag. Please keep the bag and box in which the board was shipped should the need arise to return the board.

Prior to opening the bag, place the bag near the PC into which the board will be installed. Holding the bag and the PC should dissipate any static charge that may have been created transporting the board to the PC. A static free area for installation is adviseable or use a wrist strap that is connected to the PC or to a static workstation.

1.B Memory, I/O, Interrupt, and 8/16 Bit Cycle Considerations

The 4MEG VIDEO Model 12 uses memory addresses, I/O port addresses, and an interrupt of the PC or PC/AT bus. System problems may result when the Model 12 is accessed by software if RAM is present in the memory segment that the Model 12 will occupy, if I/O ports that the Model 12 uses are used by other devices, or if the selected interrupt level is used by other PC devices. Devices that use these addresses or interrupt must either be removed, changed, or the Model 12 must be configured to avoid conflict.

The user should determine if any other peripherals in the system will interfere with the Model 12. Some 16 bit VGA graphics adapters running in 16 bit mode use memory at 0xD0000. LIM memory may also cause a conflict if it is enabled. Memory management software should be configured to avoid using the same memory segment that the Model 12 is using. The DOS program "MSD" can be used to report possible memory and I/O port conflicts. Read the "In Case of Trouble" chapter to help resolve installation problems.

Jumpers select the memory segment, I/O base address, and interrupt level. The standard base memory address is 0xD0000, the standard base I/O port address is 0x280, and the standard interrupt is IRQ level 3. 4MIP assumes these settings unless configured otherwise. Note that if the Model 12 was ordered from the factory with non-standard memory address, I/O port, or interrupt level, the board will be set with these options. To operate 4MIP with other than the standard settings, refer to the 4MIP manual for details.

The memory addresses used by Model 12 are selected by the MEM jumper. Placing the MEM jumper over the two pins marked "xD" selects the 0xD0000 thru 0xDFFFF address range. Placing the MEM jumper over the two pins marked "xE" selects the 0xE0000 thru 0xEFFFF address range. To operate 4MIP with a memory base other that 0xD0000, refer to the 4MIP manual for details.

The I/O addresses used by Model 12 are selected by the I/O jumper. Placing the I/O jumper over the two pins marked "x280" selects the 0x280 thru 0x283 address range for the I/O ports. Placing the I/O jumper over the two pins marked "x290" selects the 0x290 thru 0x293 address range for the I/O ports. To operate 4MIP with an I/O port base other that 0x280, refer to the 4MIP manual for details.

The interrupt request level is selected by two IRQ jumpers. Jumper JP12 selects one of IRQ 3, 5, 7, or 9. Jumper JP16 selects one of IRQ 10, 11, 12, 14, or 15. Note that level 2 is mapped to level 9 on the 16 bit AT bus and that interrupts higher than 9 are not available in an 8 bit PC bus slot. 4MIP can operate without using interrupts.

Refer to the **4MIP User's Manual** for details.

If the video input is from the composite video of a RS-170 camera, the standard jumper settings for the Model 12 do not need to be changed. If this is not the configuration that will be used, see the "Connections" and the "Jumpers" chapters before proceeding. Otherwise, perform the installation steps below.

1.C Installation

The 4MEG VIDEO Model 12 is packed in a static dissipative bag. Please keep the bag and box in which the board was shipped should the need arise to return the board.

Prior to opening the bag, place the bag near the PC into which the board will be installed. Holding the bag and the PC at the same time should dissipate any static charge that may have been created transporting the board to the PC. A static free area for installation is adviseable and the use of a wrist strap that is connected to the PC or to a static workstation is suggested.

1. Run MSD to check for possible I/O and memory conflicts.
2. Install 4MIP according to the instructions in the 4MIP manual.
3. Follow the directions for the PC's cover removal (if one is used with the PC) and remove the cover.
4. Locate a vacant ISA or EISA slot and remove the metal bracket and screw covering the back panel slot with which it is aligned.
5. Gently ease the imaging board into the connectors. The 4MEG VIDEO Model 12 has 16 bit bus fingers, but it can be installed in an 8 bit slot. 16 bit bus transfers will not be possible if it is installed in an 8 bit slot.
6. Replace the screw to secure the imaging board in the selected slot.
7. Connect the video input to the VIN cable.
8. Connect the GREEN cable to the monitor input or use the VGA monitor display capability of 4MIP.
9. Connect the DB25 plug on the cable into the DB25 receptacle on the Model 12.
10. Operate 4MIP and check for proper operation with the camera.
11. Perform a histogram to check for grey levels near 255 in the brightest area of the image and grey levels near 0 in the darkest area of the image. If the 255 and 0 grey levels are not achieved, adjustment of the "GAIN" and "CLMP" potentiometers may be required. See the **Gain and Black Level Adjustment** chapter.
12. Replace the PC's cover.

1.D Features

The Model 12 is a flexible image acquisition, processing, and display board for the PC or PC/AT bus. The TMS320C25 processor is available for image processing when not controlling video timing. TMS320C25 program RAM is loaded by the PC/AT and allow the processor to be programmed for specific applications. The program RAM may be replaced by ROM for stand-alone applications (no PC/AT host).

A user programmable microsequencer allows for digitization and display of video from standard video sources (RS-170, CCIR, RS-343). Video from unusual video sources such as Dalsa CL-Cx series, KODAK MEGAPLUS, and line scan cameras can also be digitized. Lines of up to 8000 pixels may be digitized. A standard Model 12 can operate with pixel clocks up to 30 MHz. Options allow pixel clocks up to 50 MHz and lines with up to 31,000 pixels.

The PC data bus interface is 16 bits wide and supports both 8 and 16 bit memory access. The Model 12 can be installed in an 8 bit PC bus slot, but will have slower memory access. The bus can run with zero wait states during image memory access for maximum throughput during image processing operations or file transfers (this may not operate on some clones).

For display, three look-up tables drive red, green and blue digital to analog converters to provide pseudo-color output. Video sync is on the green output. A cursor generator is also provided, giving a full screen cross-hair cursor, a 64 × 64 bit mapped cursor, or both. With 4MIP and 4MOBJ, a box of arbitrary size can be drawn with the cursor.

The video input is digitized to 8 bits. A DC restoration circuit clamps the input video signal to an adjustable black level. Clamping may be triggered during the video back porch or the horizontal sync, for cameras that do not provide a back porch. Potentiometers are used to adjust video gain and black level. Alternatively, connections are provided to accept 8 bit digital data or two 8 bit digital pixels for up to 16 bit input.

A sync stripper is used to detect video synchronizing signals from composite video sources and to generate a clamp signal.

The image memory starting address of each line of video is set by the TMS320. During image capture, this allows interlacing lines in the memory, which can speed up image processing operations. During display, this allows panning and scrolling of the image.

Connections are available for monochrome video input. Video outputs are green (with sync), red, and blue.

The standard Analog Module provides composite sync or horizontal sync input, vertical sync input, and pixel clock input, a TTL level trigger input for external event synchronization, a TTL level trigger output, pixel clock output, horizontal sync output, and vertical sync output.

The optional Pixel Clock and Video Four Input Multiplexer Module provides four pixel clock and video inputs. A jumper on the module allows selection of external input or external output.

1.E Related EPIX Documents

1. Camera Compatibility Guide. Lists cameras that have been interfaced to EPIX' imaging boards and have an application note or interface user manual available from EPIX.
2. PC Configuration Tips. Provides information on installation of EPIX hardware and software in the PC environment.
3. 4MIP User's Manual. Provides information on the use of 4MIP menu driven programs for the Model 12.
4. 4MOBJ Object Code Library Reference Manual and PXIPL Image Processing Object Code Library Reference Manual. Describe object code library used with the Model 12.
5. Software Directory. Third party software descriptions for use with the 4MEG VIDEO Model 12 and other EPIX products.

1.F Related Documents

1. TMS320C2x User's Guide, 1604907-9721 revision B, December 1990. Texas Instruments, Incorporated.
2. Brooktree, Graphics and Imaging Product Databook 1993. Brooktree Corporation.

2. Connectors

2.A DB25 Connector

The DB25 (D-suBminature) connector is located at the right hand edge of the Model 12. When the Model 12 is installed in a PC chassis, it is accessible at the back of the PC chassis. The connector is a female 25 pin D-Subminiature connector, AMP PN 749414-1. Eight pins are connected from the Model 12 motherboard to the DB25 (CON7). These eight pins carry video in, green out, red out, blue out and a ground pin for each of them. All other pins of the DB25 connector are connected to a 40 pin socket connector (CON6) that is located adjacent to the DB25. Some of the pins of CON6 provide power, the rest provide connections for various signals that connect to and from the Model 12. CON6 allows the pins that are not connected directly to the Model 12 motherboard to be used for purposes that are defined by the module connected to CON6.

The standard module connected to CON6 is the Analog Module. The Analog Module on the Model 12 provides the DB25 with the same signals that were on the 4MEG VIDEO Model 10 DB25 connector. An optional module that may be connected to CON6 is the Pixel Clock and Video Four Input Mux. When a module other than the Analog Module or the Pixel Clock and Video Four Input Mux Module is installed, the module's manual provides DB25 connector information.

If the only video signals required are video in, green out, red out, and blue out, or a subset of these signals, no module is required.

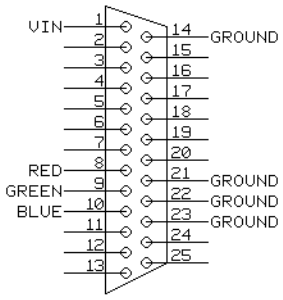

Figure 2-1. DB25 Connector - no module installed

2.A.1 Motherboard DB25 Signal Descriptions

VIN (or VIDEO IN) on pin 1 of the DB25 connector, is the analog video input. The signal level should be 1 volt peak to peak with the video portion positive and the sync tips negative. The signal input level should be 0.714 volt peak to peak if sync is not present in the video. The minimum composite video input signal that can be amplified to provide 0 thru 255 grey levels is 0.4 volts peak to peak. The maximum composite video input signal that can be amplified to provide 0 thru 255 grey levels is 2.5 volts peak to peak. The input is terminated in 75Ω to ground with the TERM (JP5) jumper. Pin 14 is the ground connection for VIN.

RED, on pin 8 of the DB25 connector, is the red video output signal of the BT453 RAMDAC. The signal level is 0 to 0.714V terminated in 75Ω to ground. Pin 21 can be used for the coaxial cable ground connection.

GREEN, on pin 9 of the DB25 connector, is the green video output signal of the BT453 RAMDAC with composite sync added. The signal level is 0 to 1V terminated in 75Ω to ground. Pin 22 can be used for the coaxial cable ground connection.

BLUE, on pin 10 of the DB25 connector, is the blue video output signal of the BT453 RAMDAC. The signal level is 0 to 0.714V terminated in 75Ω to ground. Pin 22 can be used for the coaxial cable ground connection.

2.A.2 Analog Module DB25 Signal Descriptions

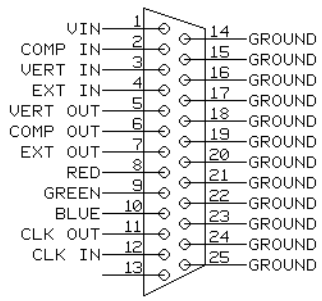

Figure 2-2. DB25 Connector - Analog Module installed

In the descriptions that follow, reference is made to jumpers and potentiometers which are described in detail in the **Jumpers and Pixel Clock Generator Module** and **Adjustments** chapters that follow.

COMP IN, on pin 2 of the DB25 connector, is the composite sync input or the horizontal sync input. This input is connected to the SSEL (JP1) jumper and the HSEL (JP7) jumper on the M12 motherboard. Signal levels are 0.286V to 4V peak to peak, with negative sync. In some applications a TTL input can be used. It is terminated in 75Ω to ground with the CSTERM (J2) jumper. Pin 15 is the ground connection for COMP IN.

VERT IN, on pin 3 of the DB25 connector, is the vertical sync input which is compared to a +1.4 volt or -1.4 volt level (selected with the VC C (J4) jumper). The voltage level should be 2.5 volts peak to peak. The input is terminated in 75Ω to ground with the VDTERM (J1). Pin 16 can be used for the coaxial cable ground connection.

EXT IN, on pin 4 of the DB25 connector, is the TTL trigger input which interrupts the TMS320C25. This signal is terminated with 330Ω to +5 volts and 390Ω to ground. This termination provides a TTL logic 1 when no signal is driving the input. A TTL high to low transition generates a level 1 interrupt to the TMS320C25. The external input allows the TMS320C25 to sense an external event such as a button press, or a part in position indicator. Pin 17 can be used for the coaxial cable ground connection.

VERT OUT, on pin 5 of the DB25 connector, is the vertical sync output. A driver provides a signal level of 0 to -4V into 75Ω. This signal is low when active. Pin 18 can be used for the coaxial cable ground connection.

COMP OUT, on pin 6 of the DB25 connector, is the composite sync output. The source of this signal is selected with J3 on the Analog Module. The source can be either from the sync generated on the Model 12 (M12 position of J3), or from the V8SYN input on the V8 connector (the V8 position of J3). When the Model 12 generated sync is selected, the signal level is 0 to -4V with a 75Ω termination to ground. When the V8 connector is selected, COMP OUT has the same level and timing as the V8SYN input. This is low when active. Pin 19 can be used for the coaxial cable ground connection.

EXT OUT, on pin 7 of the DB25 connector, is the inverted TTL output from the TMS320C25 XF pin. The external output signal is the inverted TMS320C25's external flag pin. This pin is reset and set using the SXF and RXF commands (TMS320C25 assembly language). The signal output is inverted from the sense of the software command; execution of the SXF command results in EXT OUT low; execution of the RXF command results in the EXT OUT high. The external output allows the TMS320C25 to control an external event such as a strobe flash, or a laser pulse. See the TMS320C25 User's Guide for more information on these two commands.

CLK OUT, on pin 11 of the DB25 connector, is a TTL pixel clock output buffered by a 74BCT244 on the Analog Module. Pin 23 can be used for the coaxial cable ground connection.

CLK IN, on pin 12 of the DB25 connector, is a pixel clock input, terminated in 75Ω to ground with the CKPTERM (J6) jumper. For optimal operation this should be a 50% duty cycle signal. Pin 25 can be used for the coaxial cable ground connection.

Pin 13 is not used on the Analog Module.

2.A.3 Pixel Clock and Video Four Input Mux Module DB25 Signal Descriptions

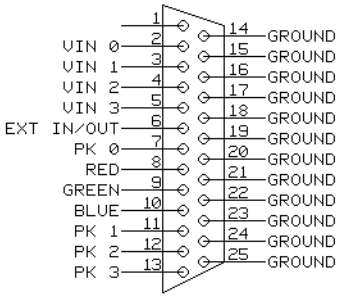

Figure 2-3. DB25 Connector - Pixel Clock and Video Four Input Mux Module installed

In the descriptions that follow, reference is made to jumpers and potentiometers which are described in detail in the **Jumpers and Pixel Clock Generator Module** and **Adjustments** chapters that follow.

VIN 0-3, on pins 2 thru 5 of the DB25 connector, are composite video inputs 0 thru 3. One of these inputs is selected to drive the video input of the Model 12. (or VIDEO IN) on pin 1 of the DB25 connector, is the analog video input. The signal level should be 1 volt peak to peak with the video portion positive and the sync tips negative. The signal input level should be 0.714 volt peak to peak if sync is not present in the video. The minimum composite video input signal that can be amplified to provide 0 thru 255 grey levels is 0.4 volts peak to peak. The maximum composite video input signal that can be amplified to provide 0 thru 255 grey levels is 2.5 volts peak to peak. The inputs are terminated in 75Ω to ground with jumpers V0-3. Pins 14 thru 17 are the ground connections for VIN 0-3.

EXT IN/OUT, on pin 6 of the DB25 connector, is selected to be either "EXT IN" or "EXT OUT" by jumper JA1. The function of the pin is as described for the Analog Module above. Pin 18 is used for the coaxial cable ground connection.

PK 0-3, on pins 7, 11, 12, and 13 of the DB25 connector, are the pixel clock inputs for VIN 0-3 respectively. They can be terminated in 75Ω to ground with jumpers K0-3. For optimal operation they should be 50% duty cycle signals. Pins 19, 23, 24, and 25 are used for the coaxial cable ground connections.

The Pixel Clock and Video Four Input Mux Module is controlled by MC0 and MC1 from the V8 connector. A PKTOV8 board with 10 position header mounts in the V8 connector. The standard chip at location B8 is replaced with one that drives the MC0 and MC1 signals in the 4 modes of operation of the V8 connector. A ten conductor cable connects to the CON1 header on the PKTOV8 board to the CON1 header on the Pixel Clock and Video Four Input Mux Module. The header at each end of the cable is wired so that the cable may be installed with either orientation.

2.B LUT Connector

The Look Up Table (LUT) connector at location A12 (also marked CON4) has a video rate 8 bit data output and an 8 bit data input. The data output is registered data from the analog to digital converter (SD7-0). The data input is to an 8 bit register (LIN7-0). The LUT connector can be used to perform real time operations on digital video such as: look up table, bit packing, or arithmetic operations. The connector provides an inverted pixel clock output, a horizontal load signal output, +5 volt power, and a ground pin for each signal pin. When a cable connection is not made to the LUT connector, a connector and small printed circuit board are installed. The board mounted connector is an AMP 10468-4. The mating connector for a cable is AMP 111196-9. It uses 40 conductor ribbon cable with conductors on 0.25 centerline spacing. The mating connector for a printed circuit board is AMP 104078-2.

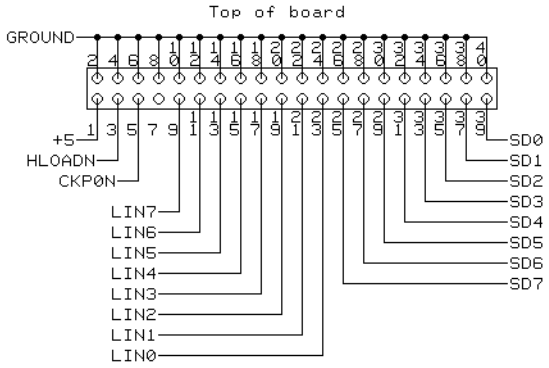

Figure 2-4. LUT Connector

2.B.1 LUT Signal Descriptions

All signals are TTL, single ended, and unterminated.

SD7 → **SD0** are the 8 registered outputs from the A-D converter. SD7 is the most significant bit.

LIN7 → **LIN0** are the 8 data inputs to the register from the LUT connector. LIN7 is the most significant bit.

HLOADN is an active low signal used to indicate the start of a horizontal line. HLOADN loads the HCM address and is driven by a GAL22V10B with 15 ns maximum propagation delay from the noninverted pixel clock. If the M12 is ordered for pixel clocks of greater than 30 MHz, an 8 ns maximum propagation GAL22V10B part is intstalled. It has three loads on the M12, and should not drive more than one load.

CKP0N is an inverted pixel clock. It has one load on the M12. A timing diagram for the LUT connector follows.

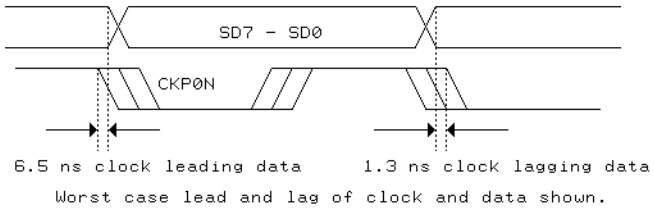

Figure 2-5. LUT Timing

2.C V8 Connector

The V8 connector at location A3 (also labelled CON3) provides bidirectional 8-bit image data to/from the image memory. The connector also provides the signals on the Model 10's Digital Interface Connector, Digital Data Interface Connector, and optional VGA Output. The board mounted connector is an AMP 10468-4. The mating connector for a cable is AMP 111196-9. It uses 40 conductor ribbon cable with conductors on 0.25 centerline spacing. The mating connector for a printed circuit board is AMP 104078-2.

Along with 8 data bits, the interface accepts or drives horizontal sync, vertical sync, and pixel clock. The 4 mode control bits are outputs. A composite sync input, V8SYN, is used to pass sync to the M12's Analog Module and if selected by jumper J3 on the Analog Module, V8SYN is connected to the composite sync output of the M12 DB25 connector.

Two bits in register T13 select one of four modes of operation for the V8 connector. The modes provide for external pixel clock, horizontal, and vertical timing from the DB25 via the Analog Module; VGA data output; data out; and data in. See the description of register T13, V8 Control 1 and 0 bits in the **Registers and Horizontal Control Memory** chapter for detailed information.

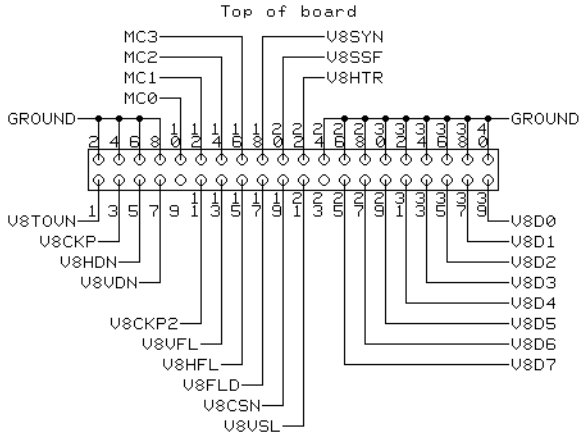

Figure 2-6. V8 Connector

2.C.1 V8 Connector Signal Descriptions

The following are unterminated, single ended, TTL signals.

V8TOVN is an active low output signal that indicates that V8D7 thru V8D0 have pixel data for display to the VGA adapter.

V8CKP is a bidirectional pixel clock.

V8HDN is a bidirectional, active low, horizontal drive signal.

V8VDN is a bidirectional, active low, vertical drive signal.

MC3, MC2, MC1, MC0 are the outputs of bits 3 thru 0 of register T12 of the TMS320C25 and are used to control cameras and digital interfaces.

V8CKP2 is a pixel clock output.

V8VFL is an active low, vertical force low output that indicates vertical blanking.

V8HFL is an active low, horizontal force low output that indicates horizontal blanking.

V8FLD is a video field output.

V8SYN is an active low, composite sync input used to drive an external monitor and to genlock the M12 during display.

V8CSN is a composite sync input used to drive an external monitor and for the M12 to genlock to for display.

V8SSF is the output of the sync stripper field signal.

V8VSL is the output of the VSPIL signal from the HCM.

V8HTR is the output of the HTRIG signal from the HCM. **V8D7 → V8D0** are the bidirectional, 8 data bits, V8D7 being the most significant bit.

V8 Connector timing diagrams are shown below for pixel clock, data, horizontal, and vertical inputs and outputs.

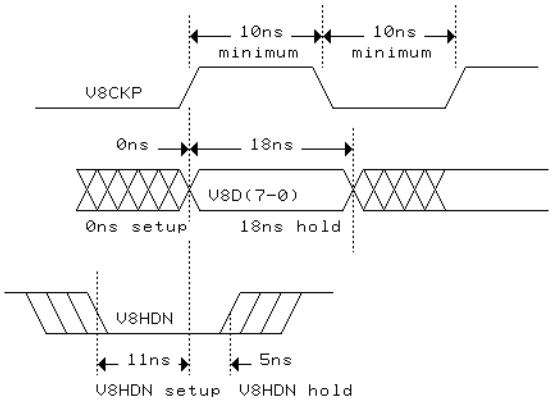

Figure 2-7. V8 Connector Pixel Clock, Data, and Horizontal Input Timing

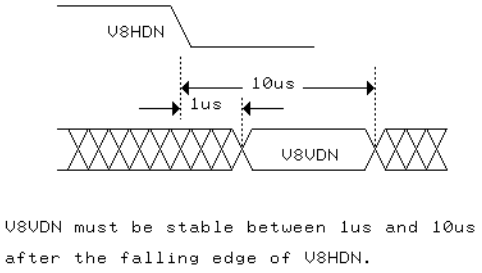

Figure 2-8. V8 Connector Horizontal and Vertical Input Timing

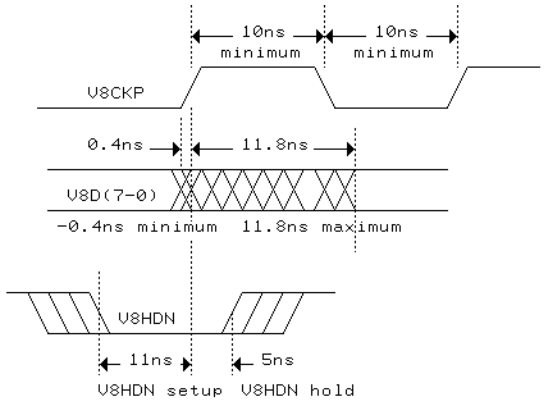

Figure 2-9. V8 Connector Pixel Clock, Data, and Horizontal Output Timing

3. Jumpers and Pixel Clock Generator Module

3.A Motherboard Standard Jumper Settings

Prior to shipping the 4MEG VIDEO Model 12 to customers, EPIX configures the jumpers on the motherboard and the Analog Module or Pixel Clock and Video Four Input Multiplexer Module to the standard positions listed in Tables 3-1, 3-2, and 3-3. With the jumpers in these positions the Model 12 is configured to genlock to a composite RS-170 or CCIR video source terminated in 75 ohms. Note that it is assumed that the user is facing the component side of the board with the PC bus fingers pointing down. Block diagrams are shown for the analog section jumpers and potentiometers, and for the other jumpers in this section. If the Model 12 is configured with a different module than the Analog Module or Pixel Clock and Video Four Input Multiplexer (4PVINAM) Module, consult the module's manual for additional configuration information.

Label	Jumper	Position	Mark	Comment
SSEL	JP1	Right	V	Video input to sync stripper.
MEM	JP4	Left	D	Decode PC bus 0xD segment for memory.
TERM	JP5	On Both Pins		Video input terminated in 75 ohms to ground.
PCLK	JP6	Left	B	Master mode pixel clock is PC bus 14.318 MHz.
HSEL	JP7	Right	S	Genlock to composite sync from sync stripper.
0WS	JP10	On one pin		Disable PC bus 0 wait states.
IRQ	JP12	Left	3	Select IRQ3 interrupt.
I/O	JP13	Right	x280	Select 0x280 as PC bus I/O base address.
CLMP	JP15	Left	M	Video clamped by sync stripper or programmable clamp.
DCC1		On one pin		DC restoration used.
DCC2		On one pin		DC restoration used.

TABLE 3-1. Motherboard Standard Jumper Settings

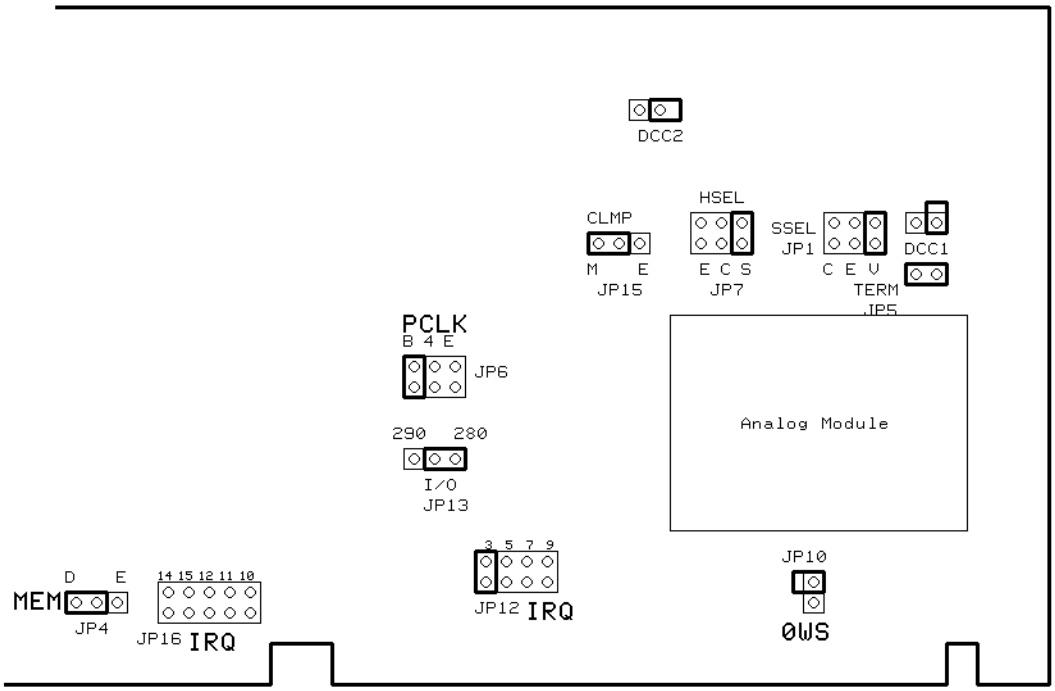

Figure 3-1. Motherboard Jumper Locations and Standard Settings

3.B Motherboard Jumper Descriptions

SSEL JP1 selects one of three inputs to the sync stripper: composite video input from the DB25 connector, composite sync from the V8 connector, composite sync input from the Analog Module and the DB25 connector. The selected signal is connected to the sync stripper input.

SSEL Position	Mark	Select
Left	C	Analog Module composite input from DB25 pin 2.
Middle	E	V8SYN from pin 18 of the V8 connector.
Right	V	Composite video input from DB25 pin 1.

MEM JP4 selects the memory base address on the PC bus. The base address is 0xE0000 or 0xD0000, unless specified otherwise when ordering. If a different base address has been requested, the socketed IC at K13 (to the right of the MEM jumper) will be marked with the two addresses.

MEM Position	Mark	Memory base address.
Left	D	0xD0000
Right	E	0xE0000

TERM JP5 terminates the video input in 75 ohms to ground. Installing the jumper on one pin and leaving the other pin unconnected selects a high impedance (9K ohms) which is used when another device terminates the video input.

TERM Position	Termination
On both pins	75 ohms to ground.
On one pin	High impedance (9K ohms to ground).

PCLK JP6 is used to select the pixel clock source when the Model 12 is in master sync mode (generating video timing).

PCLK Position	Mark	Master mode pixel clock.
Left	B	PC Bus 14.318 MHz.
Middle	4	Pixel clock generator module.
Right	E	V8 or Analog Module and DB25.

HSEL JP7 is used to select the horizontal or sync source *when the Model 12 is genlocked or when using an external pixel clock*, and selects the sync source for the programmable video timing detector. The source can be the sync stripper, COMP IN from the DB25 connector thru the Analog Module, or V8HDN from the V8 connector.

Select the "S" position (sync stripper output) with HSEL JP7 if timing information is to be derived from composite video or composite sync and when using a camera pixel clock with composite video as the sync source.

Select the "E" position of HSEL JP7 when the video timing source is the V8 connector.

Select the "C" position of HSEL JP7 when a TTL level composite sync or horizontal sync is connected to the DB25 COMP IN signal thru the Analog Module.

HSEL Position	Mark	Horizontal or sync source.
Left	E	V8HDN from V8 connector.
Middle	C	COMP IN from DB25 thru Analog Module.
Right	S	Sync stripper output.

0WS JP10 connects to the PC bus No Wait State line and shortens PC bus accesses to image memory. Zero wait states may not work on some PCs.

0WS Position	Select
On both pins	Zero wait states.
On one pin	Normal bus operation.

IRQ JP12 (and JP16) are used to select an interrupt on the PC bus. The positions are marked "3 5 7 9" and select one of the respective interrupts on the PC bus for use by the Model 12. Note that level 9 appears as level 2 in an 8 bit PC bus slot and note that interrupts higher than 9 are not available in an 8 bit PC bus slot.

IRQ Position	Mark	Select
Left	3	IRQ3
2nd from left	5	IRQ5
3rd from left	7	IRQ7
4th from left	2	IRQ9 (IRQ2 in 8 bit slot)
5th from left	10	IRQ10
6th from left	11	IRQ11
7th from left	12	IRQ12
8th from left	15	IRQ15
9th from left	14	IRQ14

IRQ JP16 (and JP12) are used to select an interrupt on the PC bus. The positions are marked "14 15 12 11 10" and select one of the respective interrupts on the PC bus for use by the Model 12. Note that interrupts higher than 9 are not available in an 8 bit PC bus slot.

IRQ Position	Mark	Select
Left	3	IRQ14
2nd from left	5	IRQ15
3rd from left	7	IRQ12
4th from left	2	IRQ11
5th from left	10	IRQ10

The **I/O** jumper selects one of two base addresses for the four PC bus registers. The base I/O addresses are 0x280 or 0x290. Should the user request alternate I/O addresses, the socketed logic chip up and to the left of the I/O jumper will be labelled with the two addresses. The left jumper position will select the upper address.

I/O Position	Mark	Select
Left	x290	0x290 base address.
Right	x280	0x280 base address.

The **CLMP JP15** jumper selects one of three signals to clamp the video input signal from the DB25 connector. The left position (marked M) selects either the programmable HCM based clamp signal (T13, SYCL = 1) or the sync stripper burst signal as the clamp signal (T13, SYCL = 0). The right position (marked E) selects the signal selected by the HSEL (JP7) jumper. Leaving the jumper on just one of the three pins allows the clamp signal to be pulled to a logic 1 and not clamp the video input. This position is selected when the video input is DC coupled (see DCC1 and DCC2 jumper descriptions).

CLMP JP15 Position	Mark	Select
Left	M	Sync stripper or HCM clamp.
Right	E	HSEL selected signal for clamp.

DCC1 & DCC2 jumpers short two capacitors used in the DC restoration circuit. These jumpers should be placed on just one pin to allow DC restoration. When it is desired to use a camera with a DC coupled video output, the jumpers can be placed over both pins and the **CLMP JP15** jumper placed on just one pin. Adjustment of the **GAIN** potentiometer may be required. See the **Gain and Black Level Adjustment** chapter for details.

DCC1 & DCC2 Position	Select
On both pins	DC coupled.
On one pin	DC restoration.

A block diagram of the analog input potentiometers and jumpers is shown in Figure 3-2.

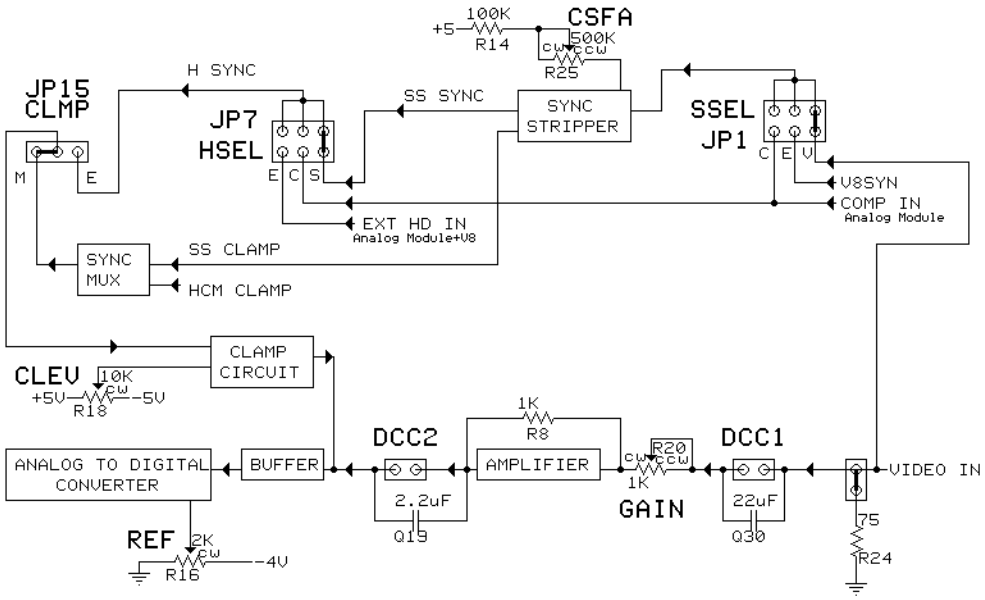

Figure 3-2. Analog Input Potentiometers and Jumpers Block Diagram

A block diagram of the other jumpers on the Model 12 motherboard is shown in Figure 3-3.

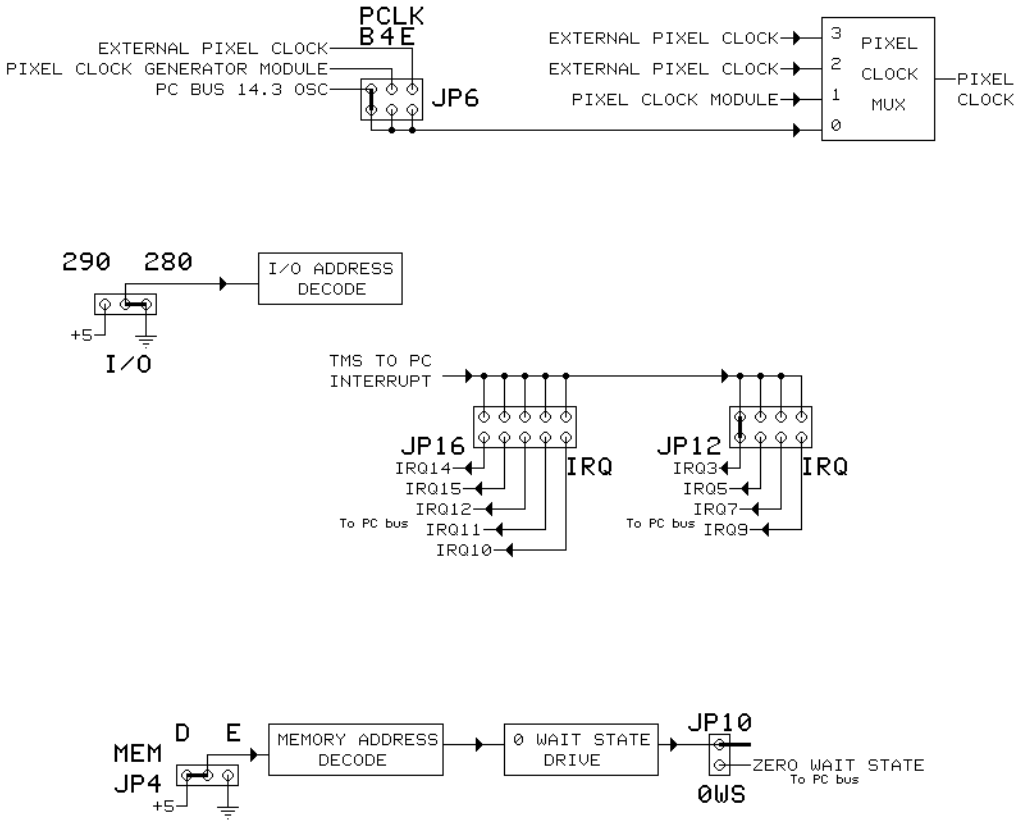

Figure 3-3. Other Motherboard Jumpers

3.C Analog Module Standard Jumper Settings

Prior to shipping the 4MEG VIDEO Model 12 to customers, EPIX configures the jumpers on the Analog Module to the standard positions listed in the table below and shown in Figure 3-4. A jumper schematic diagram for the Analog Module is shown at the end of this section. See the section on the 4PVINAM Module for a description of the jumpers on that module.

Label	Jumper	Position	Mark	Comment
VDTERM	J1	On both pins		Video drive input terminated in 75 ohms to ground.
CSTERM	J2	On both pins		Composite sync input terminated in 75 ohms to ground.
	J3	M12		Composite sync output from Model 12.
VD C	J4	Left	-	Vertical drive input compared to -1.4V.
CK	J5	Left	1.4	Pixel clock input compared to +1.4V.
CKPTERM	J6	On both pins		Pixel clock input terminated in 75 ohms to ground.

TABLE 3-2. Analog Module Standard Jumper Settings

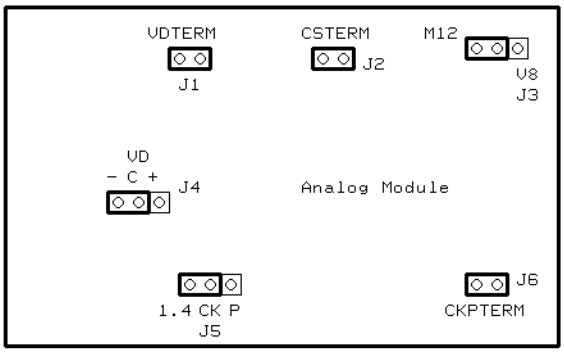

Figure 3-4. Analog Module Jumper Locations and Standard Settings

3.D Analog Module Jumper Descriptions

VDTERM J1 terminates the vertical drive input of the DB25 connector in 75 ohms to ground when installed on both pins. Placing the jumper on just one pin removes the 75 ohm termination and prevents the jumper from being lost. The termination is removed when more than one device is driven by a vertical drive source.

VDTERM Position	Select
On both pins	Terminate vertical drive input in 75 ohms to ground.
On one pin	Remove 75 ohm termination.

CSTERM J2 terminates the composite sync input of the DB25 connector in 75 ohms to ground when installed on both pins. Placing the jumper on just one pin removes the 75 ohm termination.

CSTERM Position	Select
On both pins	Terminate composite sync input in 75 ohms to ground.
On one pin	Remove 75 ohm termination.

OUTCS J3 selects the source of composite sync output to the DB25 connector from either the M12 composite sync circuit or from the V8SYN signal on the V8 connector. The V8SYN signal is used when digitizing from the Kodak MEGAPLUS digital interface. When V8SYN is a sync source for the board to genlock to in display mode, and to drive the video monitor while digitizing, it prevents the monitor from losing sync.

OUTCS J3 Position	Mark	Select
Left	M12	M12 sync circuit drives composite sync output.
Right	V8	V8SYN used to drive composite sync output.

VD C J4 selects the voltage used for comparison to the DB25 connector vertical drive input. Some video systems use a vertical drive signal that is +4 volts when not in vertical drive and 0 volts during vertical drive. Some video systems use a vertical drive signal that is 0 volts when not in vertical drive and -4 volts during vertical drive. The two jumper positions select either a positive or negative 1.4 volt signal as the voltage for the vertical drive comparator. The comparator output is read by the TMS320C25 to determine when vertical drive occurs. It is also used with the DB25 horizontal input to create composite sync when the Model 12 is driven with separate external vertical and horizontal drive.

Note that the negative position should be selected when using an external pixel clock and not using external vertical drive.

VD C Position	Mark	Select
Left	-	Negative 1.4 volt for comparison to vertical drive input.
Right	+	Positive 1.4 volt for comparison to vertical drive input.

CK J5 selects the voltage used for comparison of the DB25 connector pixel clock input. The two jumper positions select either a positive 1.4 volt signal or a potentiometer for comparison to the pixel clock input. The 1.4 volt position can be used with a pixel clock that has TTL levels. Some camera pixel clock outputs do not have TTL levels. See the **Adjustments** chapter for details.

CK Position	Mark	Select
Left	1.4	Positive 1.4 volt for comparison of pixel clock input.
Right	P	Potentiometer for comparison of pixel clock input.

CKPTERM J6 terminates the DB25 pixel clock input in 75 ohms to ground. Installing the jumper over a single pin removes the 75 ohm input termination.

CKPTERM Position	Select
On both pins	Pixel clock input terminated in 75 ohms to ground.
On one pin	Pixel clock termination removed.

A block diagram of the analog module potentiometers and jumpers is shown in Figure 3-5.

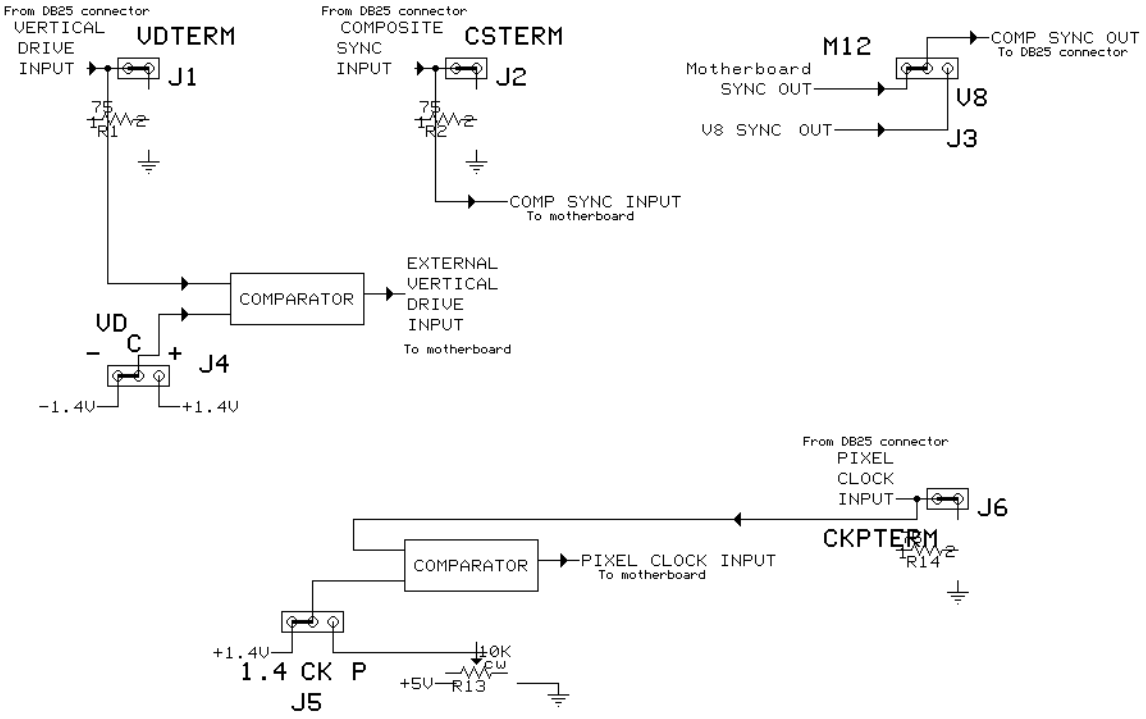

Figure 3-5. Analog Module Potentiometers and Jumpers Block Diagram

3.E Pixel Clock and Video Four Input Multiplexer Jumper Settings

Prior to shipping the 4MEG VIDEO Model 12 to customers, EPIX configures the jumpers on the Pixel Clock and Video Four Input Multiplexer Module (4PVINAM) to the standard positions listed in the table below and shown in Figure 3-6. A jumper schematic diagram for the 4PVINAM Module is shown at the end of this section.

Label	Jumper	Position	Mark	Comment
V0		On both pins		Video input 0 terminated in 75 ohms to ground.
V1		On both pins		Video input 1 terminated in 75 ohms to ground.
V2		On both pins		Video input 2 terminated in 75 ohms to ground.
V3		On both pins		Video input 3 terminated in 75 ohms to ground.
K0		On both pins		Pixel clock 0 input terminated in 75 ohms to ground.
K1		On both pins		Pixel clock 1 input terminated in 75 ohms to ground.
K2		On both pins		Pixel clock 2 input terminated in 75 ohms to ground.
K3		On both pins		Pixel clock 3 input terminated in 75 ohms to ground.
	J5	Right	1.4	Pixel clock input compared to +1.4V.
IN	JA1	Left	OUT	External input to Model 12 motherboard.

TABLE 3-3. Pixel Clock and Video Four Input Multiplexer Jumper Settings

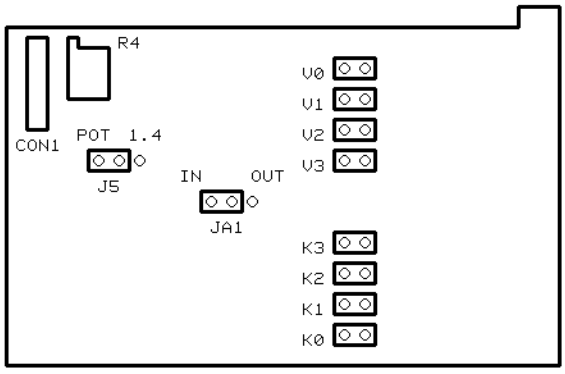

Figure 3-6. Pixel Clock and Video Four Input Multiplexer Jumper Locations

3.F Pixel Clock and Video Four Input Multiplexer Jumper Descriptions

V0-V3 terminates the video input 0 to 3 from the DB25 connector in 75 ohms to ground when installed on both pins. Placing the jumper on just one pin removes the 75 ohm termination and prevents the jumper from being lost. The termination is removed when the video input is not at the end of a coaxial cable.

V0-V3 Position	Select
On both pins	Terminate vertical drive input in 75 ohms to ground.
On one pin	Remove 75 ohm termination.

K0-K3 terminates pixel clock input 0 to 3 from the DB25 connector in 75 ohms to ground when installed on both pins. Placing the jumper on just one pin removes the 75 ohm termination and prevents the jumper from being lost. The termination is removed when the pixel clock input is not at the end of a coaxial cable.

K0-K3 Position	Select
On both pins	Terminate pixel clock input in 75 ohms to ground.
On one pin	Remove 75 ohm termination.

CK selects the comparison voltage for the pixel clock to be either a +5 to 0 volt signal from potentiometer R1 or a fixed 1.4 volt signal. The 1.4 volt position can be used with a pixel clock that has TTL levels. Some camera pixel clock outputs do not have TTL levels. See the **Adjustments** chapter for details.

CK Position	Mark	Select
Left	POT	Potentiometer for comparison of pixel clock input.
Right	1.4	Positive 1.4 volt for comparison of pixel clock input.

JA1 selects pin 6 of the DB25 connector to be either an external input or an external output.

JA1 Position	Mark	Select
Left	IN	External input selected.
Right	OUT	External output selected.

A block diagram of the Pixel Clock and Video Four Input Multiplexer is shown in Figure 3-7.

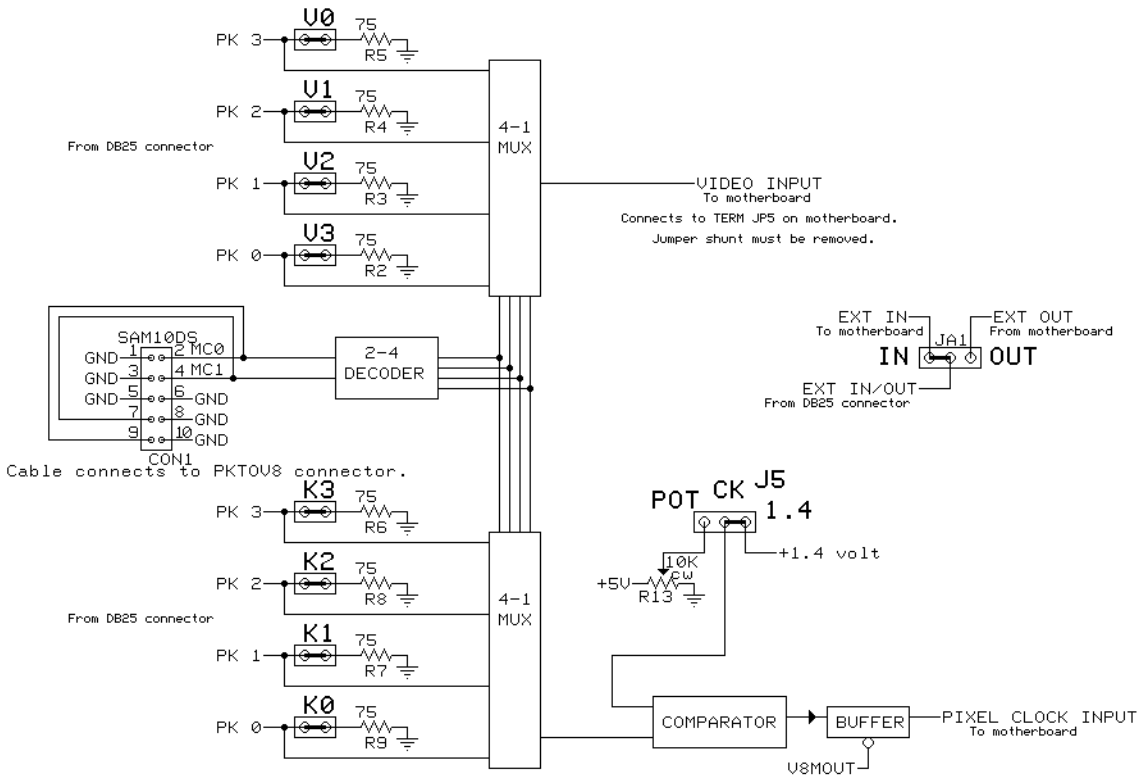

Figure 3-7. Pixel Clock and Video Four Input Multiplexer Jumpers Block Diagram

Selection of the video and pixel clock input is controlled by the T12 register bits MC1 and MC0 as shown in the table below. In 4MIP the mode control bits (MC) may be controlled by the *Camera Control Mode* in the *Video Capture & Display* menu of the *Capture* menu. On startup of 4MIP the bits are set to 0.

MC1	MC0	Video Input and Pixel Clock Selected
1	1	VIN 3, PK 3
1	0	VIN 2, PK 2
0	1	VIN 1, PK 1
0	0	VIN 0, PK 0

TABLE 3-4. Pixel Clock and Video Four Input Multiplexer Selection

To keep cross coupling of one video input to another to a minimum, it is recommended that the video inputs to the Pixel Clock and Video Four Input Multiplexer are synchronized. In other words, the video sources should have identical vertical and horizontal timing.

3.G Pixel Clock Generator Module

The blue, socketed module with white alphanumerics at location F7 is the pixel clock generator module (PCGM). While not a jumper, the PCGM may be user installed, similar to a jumper.

The standard Model 12 is shipped with a STTLPCGM-107 PCGM which generates a frequency of 14.318 MHz. The "S" prefix denotes that the TTL PCGM is a special frequency. The PCGM is available in standard frequencies

from 2 MHz to 10 MHz in 0.5 MHz increments, and from 10 MHz to 30 MHz in 1 MHz increments. Some of the special frequencies available are shown in Table 3-5.

Note that the PCGM is static sensitive and should be removed or installed by following static handling procedures.

A 30 MHz Model 12 can use any frequency PCGM equal to or less than 30 MHz. Similar frequency rules apply to higher frequency Model 12 boards. If square pixels are desired from a RS-170 video source, a 12 MHz PCGM is recommended.

Clock Frequency	PCGM Part Number
9.204 MHz	STTLPCGM-122
9.752 MHz	STTLPCGM-109
11.45 MHz	STTLPCGM-129
12.5 MHz	STTLPCGM-117
13.3 MHz	STTLPCGM-110
14.318 MHz	STTLPCGM-107
21.4 MHz	STTLPCGM-124
28.6 MHz	STTLPCGM-250
33.33 MHz	STTLPCGM-121
35.0 MHz	STTLPCGM-120
40.0 MHz	STTLPCGM-130
45.0 MHz	STTLPCGM-131
50.0 MHz	STTLPCGM-139

TABLE 3-5. Special PCGM Clock Frequencies and Part Numbers

4. Adjustments

4.A Motherboard Potentiometers

The 4MEG VIDEO Model 12 motherboard has five potentiometers. They adjust the input video gain, video clamp level, A-D reference voltage level, the sync stripper horizontal frequency detection, and when pixel clocks greater than 40 MHz are used, the hysterisis of the A-D converter.

A procedure to adjust the video gain and clamp (black) level is given in the **Gain and Black Level Adjustment** chapter of this manual.

Motherboard potentiometer locations are shown in Figure 4-1.

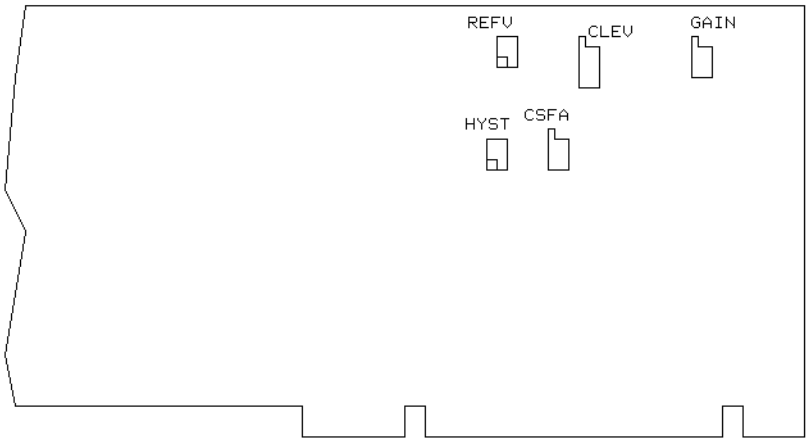

Figure 4-1. Motherboard Potentiometer Locations

The **GAIN** pot is used to adjust the gain of the video input amplifier. Turning the GAIN pot clockwise will increase the gain. The video input of the analog to digital converter (A-D) Analog Devices AD9048, is pin 21 with ground on pin 25. An axial capacitor marked "AGND" provides ground on both legs at location A16. For the Analog Devices AD9012 A-D, the video input is pin 5, with ground on pin 2. The input signal should be from 0 to -2V measured from the back porch of the video to maximum white level.

The **CLEV** (Clamp LEVel) pot is used to adjust the voltage that the video is clamped to on the video back porch. The voltage of the video back porch (between the end of horizontal drive and the beginning of active video) should be set so that the blackest portion of the video input has a 0 grey level. Turning CLEV clockwise makes the clamp voltage more positive and shifts the video input towards the zero grey level.

The **REFV** (REFerence Voltage) pot is used to adjust the A-D 255 grey level reference voltage. Damage to the A-D converter may take place if the reference voltage is more negative than -2.2 volts. It is normally set to -2.0 volts. Adjustment of this setting is **not recommended** and normally not required. Pin 26 of the AD9048 is the reference voltage of the A-D. The reference voltage determines the maximum white level and is the upper limit of the range of the A-D.

The **CSFA** (Composite Sync Frequency Adjust) pot is used to adjust the sync stripper's clamp width, vertical drive width, and field detector. When genlocking to an interlaced video format, 4MIP allows display of the decoded video

field which can be used to determine when the CSFA pot is adjusted properly. Turning the CSFA pot clockwise sets the sync stripper for lower horizontal frequency video formats.

A programmable method of decoding the horizontal and vertical timing information and clamping the video input is available in the Video Format menu of the 4MIP software for the Model 12. The menu item is called *Genlock Sync and Clamp: HCM* and it appears in the *Custom Interface Modes* menu of the *Digitize Video Format* menu and the *Display Video Format* menu of the *Video Format & Resolution* menu of the *Setup* menu of 4MIP version 2.8.

The **HYST** potentiometer is used to adjust the hysterisis of the AD9012 A-D converter. This pot does not normally require adjustment and only has a connection to the AD9012 which is used for pixel clock rates greater than 40 MHz.

4.B Analog Module Potentiometer

The Analog Module has a potentiometer to adjust the comparison voltage for the Analog Module external pixel clock input comparator. The CK jumper on the Analog Module must be in the "P" position for the potentiometer voltage to be used. Turning pot clockwise makes the comparison voltage more negative. The range of adjustment is +5 volts (CCW) to ground (CW). Adjust the potentiometer for optimum slicing of the external pixel clock input.

4.C Pixel Clock and Video Four Input Multiplexer Module Potentiometer

The Pixel Clock and Video Four Input Multiplexer Module has a potentiometer to adjust the comparison voltage for the module's external pixel clock input comparator. It performs the same function as does the pot on the Analog Module (above). The CK jumper (J5) on the module must be in the "POT" position for the potentiometer voltage to be used. Turning pot clockwise makes the comparison voltage more negative. The range of adjustment is +5 volts (CCW) to ground (CW). Adjust the potentiometer for optimum slicing of the external pixel clock input. Note that there is only one pot for the four pixel clock inputs which implies that the four pixel clock input voltage levels are similar.

5. Architecture

5.A Data Path

The diagram below shows the data path connections of the logic blocks of the 4MEG VIDEO Model 12. The block functions are described in the following text.

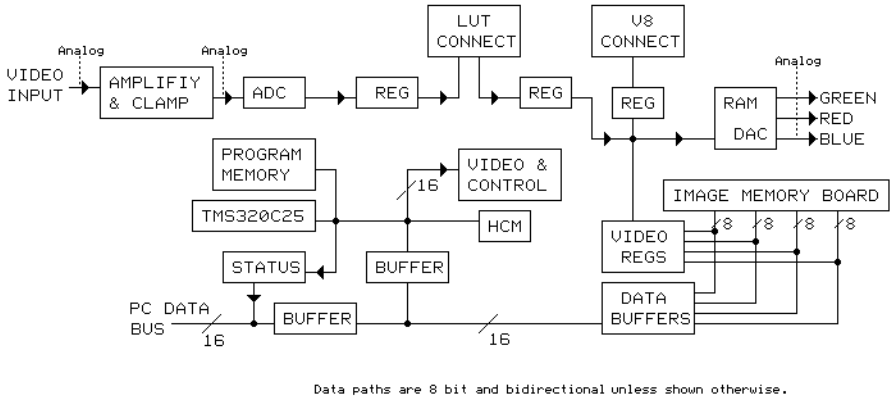

Figure 5-1. Data Path Block Diagram

5.A.1 AMPLIFY & CLAMP

The AMPLIFY & CLAMP circuits buffer, amplify, and clamp the video input. Gain and clamp level are set with potentiometers.

5.A.2 ADC

The ADC (Analog to Digital Converter) converts the analog video signal to an 8 bit code on each pixel clock. The output of the ADC is connected to a register (REG) to provide additional drive capability and to allow the output to the LUT connector to be tristated.

5.A.3 LUT CONNECT

To allow look up table transformations or other video rate operations, the registered ADC output connects to the LUT connector. The input from the LUT connector is registered to provide addition drive and to allow the LUT connector input to be tristated when not in digitize mode.

5.A.4 V8 CONNECT

The V8 connector provides connections for 8 bit digital video input, output, and control signals.

5.A.5 RAMDAC & CURSOR

A set of three 256 byte look up tables (RAM) transform the 8 bit digital data into up to 2 to the 24th colors. The 24 bit output of the look up tables connect to three 8 bit digital to analog converters (DAC). Each of the DACs drive one of the GREEN, RED, or BLUE outputs of the DB25 connector. The cursor allows the video to be overlaid with a programmable size crosshair and/or a 64 by 64 one bit icon. The RAM and CURSOR are loaded by the TMS320C25.

5.A.6 VIDEO REGS

The video registers allow four sequential 8 bit pixels to be loaded while the previous four pixels are written to image memory when in digitize mode. In display mode, the video registers allow four sequential 8 bit pixels to be loaded from the image memory and driven to the video bus 8 bits at a time.

5.A.7 IMAGE MEMORY BOARD

The image memory is triple ported to the PC/AT bus, to the TMS320C25, and to video data (ADC input thru the LUT, RAMDAC output, and V8 connector).

5.A.8 DATA BUFFERS

The data buffers provide byte or word access to either the PC/AT bus or the TMS320C25.

5.A.9 TMS320C25

A 50 MHz Texas Instruments TMS320C25 digital signal processor is used to control the operation of the Model 12, to perform image processing operations, and to control the generation of the video format.

5.A.10 PROGRAM MEMORY

A 32K × 16 bit static RAM program memory provides zero wait state instruction access by the TMS320C25. The PC/AT bus passes data to and from the TMS320C25 via the program memory. To allow the PC/AT bus to access image memory while the TMS320C25 executes instructions, a buffer separates the TMS320C25 and program memory from the 16 bit bus to the PC/AT buffer and to the image memory data buffers. When the PC/AT bus is accessing the TMS320C25's program memory, wait states are generated on the PC/AT bus until the TMS320C25 enters the "HOLD ACKNOWLEDGE" state.

5.A.11 STATUS

A status register is provided to allow the TMS320C25 to pass information to the PC/AT bus without disturbing the TMS320C25 data path to image memory.

5.A.12 HCM

The Horizontal Control Memory (HCM) is written by the TMS320C25 with data that generates video control signals. The HCM is addressed by a counter which is incremented by the pixel clock. The registered outputs of the HCM are connected to logic devices which control data flow to and from the image memory. The HCM interfaces with the VIDEO CONTROL logic which consists of the following elements:

5.A.12.a Vertical Control Register The TMS320C25 uses the Vertical Control Register (VCR) to generate video timing signals that take place at horizontal or twice horizontal rates, such as, vertical blanking, vertical refresh, vertical sync, and the field signal. The VCR and HCM generate video sync signals.

5.A.12.b Video Address Counter A 24 bit counter generates image memory addresses during digitize and display. The counter is loaded by the TMS320C25 usually during horizontal blanking. The counter is incremented or decremented after or prior to each image memory cycle which is a maximum of every four pixels.

5.A.12.c Sync Logic Composite sync may be generated by the Model 12 or may be received from a video source. The HCM and the sync logic can be used to detect vertical sync and field timing from a composite sync or composite video input.

5.A.12.d Sync Stripper When genlocking to composite video, composite sync, or horizontal sync, the sync stripper is used to detect video synchronization signals. It separates and regenerates horizontal, vertical, and field information from the composite input signal. It also generates a clamp signal to DC restore the video signal at the start of each line.

5.A.12.e Pixel Clock Generator A register and jumper select the pixel clock to be either the PC bus 14.318 MHz oscillator, an externally supplied clock, or a plug-in 2 MHz to 50 MHz pixel clock generator module.

6. Registers and Horizontal Control Memory

Two register sets are described below. The 8 bit PC Bus I/O registers are in the PC processor I/O space. The 16 bit TMS320 I/O registers are in the TMS320 I/O space. Bits shown as "reserved" should be written with zero and masked on a read.

6.A PC Bus I/O Registers

The "I/O" jumper selects either 0x280 or 0x290 as the PC bus I/O base address. The PC registers below are shown with 0x280 as the base address. The I/O address decode circuit can be replaced to provide other I/O base selections.

0x280 (PC0) TMS320 Status Register. Read Only. Undefined at power up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3-7	T3-6	T3-5	T3-4	T3-3	T3-2	T3-1	T3-0

Status register PC0 is written by the TMS320 as register T3. If an interrupt to the PC was enabled and waiting, a read of PC0 clears the interrupt.

0x281 (PC1). TMS320 Status Register. Read Only. Undefined at power up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3-7	T3-6	T3-5	T3-4	T3-3	T3-2	T3-1	T3-0

A read of PC1 is similar to reading PC0 but does not clear a waiting interrupt. This allows the status to be read while interrupts are operational.

0x281 (PC1). PC Control Register. Write Only. Cleared at power-up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCME	PCIM	PC5	PCIMA	PCENI	PCIT	PCTRUN	PC0

Bit 7 → PC Memory Enable
1 → Decode PC bus memory addresses (image memory or program memory).
0 → No Decode of PC bus memory addresses.

Bit 6 → PC Image Memory
1 → Image memory selected.
0 → Program memory selected.

Bit 5 → PC5
1 → T0 register bit 4=1.
0 → T0 register bit 4=0.

Bit 4 → PC Image Memory Access
1 → PC Image Memory Access (when T12 bit 4 = 0).
0 → TMS320 may have access.

Bit 3 → PC ENable Interrupt
1 → Enable TMS320 to PC interrupt.
0 → No interrupts to PC.

Bit 2 → PC Interrupt TMS320
1 → Interrupt to TMS320 on low to high transition.
0 → No interrupt to TMS320.

Bit 1 → PC TMS320 RUN
1 → Allow TMS320 to execute instructions.
0 → Reset TMS320 (low for ≥300 ns).

Bit 0 → PC to TMS320 T0 Register Signal (T0 bit 9)
1 → T0 register bit 9=1.
0 → T0 register bit 9=0.

0x282 (PC2). Lower Memory Offset Register (LMO). Read/Write. Undefined at power-up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MO7	MO6	MO5	MO4	MO3	MO2	MO1	MO0

0x283 (PC3). Upper Memory Offset Register (UMO). Read/Write. Undefined at power-up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MO15 MS1 16MB	MO14 MS0 16MB	MO13 MS1 4MB	MO12 MS0 4MB	MO11 MS1 1MB	MO10 MS0 1MB	MO9	MO8

To access more than the first 64K of image memory, the PC uses a 16 bit memory offset register (MO) consisting of the UMO and LMO. The MO is shared with the TMS320. The PC can read or write the contents of the LMO or UMO register only when the PC (and not the TMS320) has access to the image memory. The contents of the MO register is added to bits 15 and 14 of the PC address to create the upper address bits to the image memory.

When the Model 12 is connected to an IMAGE MEMORY EXPANSION board, two bits of the UMO are used to select one of four groups of four memory modules on the IMAGE MEMORY EXPANSION board. A carry from the lower bits of the address does not affect the module select bits. When 16MB modules are installed, MO15 and MO14 select one of four groups of four memory modules. When 4MB modules are installed, MO13 and MO12 select one of four groups of four memory modules. When 1MB modules are installed, MO11 and MO10 select one of four groups of four memory modules.

6.B TMS320 I/O Registers

0x0 (T0) PC and Video Status Register. Read Only. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						PCB0	P16C	NSVD	SODD	EVD	PCB5	Reserved			

Bit 9 → PCB0
- 1 → PC1 register bit 0 (PCB0) = 1.
- 0 → PC1 register bit PCB0 = 0.

Bit 8 → P16C
- 1 → PC bus 16 bit bus memory cycles available.
- 0 → PC bus 8 bit bus cycles.

Bit 7 → NSVD
- 1 → Not vertical drive from sync stripper or sync detect (selected by SYCL, T13).
- 0 → Vertical drive from sync stripper or sync detect.

Bit 6 → SODD
- 1 → Odd field from sync stripper or sync detect (selected by SYCL, T13).
- 0 → Even field from sync stripper or sync detect.

Bit 5 → EVD
- 1 → External vertical drive from V8 or DB25 connector = 1.
- 0 → Vertical drive from V8 or DB25 connector = 0.

Bit 4 → PCB5
- 1 → PC1 register bit 5 (PCB5) = 1.
- 0 → PC1 register bit PCB5 = 0.

Register T0 can be used by TMS320 software to determine the state of vertical sync, video field, and the state of bits 5 and 0 of register PC1. The sync stripper vertical sync may be selected to be from either the sync stripper or an on-board programmable vertical sync and field detector. The programmable vertical sync and field detector is selected with bit 3 of register T13 (SYCL). The field signal is selected from either the sync stripper or the on-board programmable vertical sync and field detector. Bits PCB5 and PCB0 from register PC1 provide communication between the PC and the TMS320.

0x0 (T0) Interrupt PC. Write Only.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Don't care.															

Writing to T0 when PC interrupts are enabled generates an interrupt to the PC.

0x1 (T1) Control Register 1. Write Only. Cleared at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MEMS	HLLE	HS1K	HCME	HCMG	PHS0	ADS1	ADS0	HS16K	HS4K	PHS1	UNBK	Rsvd	Rsvd	Rsvd	DEC

Bit	15	→	MEMory Select	
	1	→	Select image memory.	
	0	→	Select horizontal control memory.	
Bit	14	→	HCM starting address Load on Leading Edge	
	1	→	Load HCM start addr. on leading edge of input sync when in genlock mode.	
	0	→	Load HCM start addr. on trailing edge of input sync when in genlock mode.	
Bit	13	→	Horizontal Starting address 1K	
			-see bits 7 and 6 below	
Bit	12	→	HCM Enable	
	1	→	Enable HCM counters.	
	0	→	Disable HCM counters, and load HCM counters with starting address.	
Bit	11	→	Horizontal Control Memory Gate	
	1	→	HCM SMC to image memory allowed.	
	0	→	HCM SMC to image memory not allowed.	
Bit	10	→	Pixel clock and Horizontal load Select 0	
			-see bit 5 below	

Bit	9	8	→	Address Select 1, 0	
	0	0	→	RAMDAC Addr Register and Cursor Addr Register 0.	
	0	1	→	RAMDAC Color Palette RAM and Cursor Addr Register 1.	
	1	0	→	RAMDAC Addr Register and Cursor RAM.	
	1	1	→	RAMDAC Overlay Register and Cursor Control Register.	

Bit	13	7	6	→	Horizontal control memory Starting Address
	0	0	0	→	0 (0x0000)
	0	0	1	→	1024 (0x0400)
	0	1	0	→	4096 (0x1000)
	0	1	1	→	5120 (0x1400)
	1	0	0	→	16384 (0x4000)
	1	0	1	→	17408 (0x4400)
	1	1	0	→	20480 (0x5000)
	1	1	1	→	21504 (0x5400)

	PHS1	PHS0		
Bit	5	10	→	Pixel clock and Horizontal load Select 1 and 0
	0	0	→	PC bus 14.318 MHz clock and HCM load (master).
	0	1	→	Pixel Clock Gen. Module (PCGM) clock and PCGM load (genlock).
	1	0	→	Pin 1 of DIC clock and HCM load (external 0).
	1	1	→	Pin 1 of DIC clock and pin 9 of DIC load (external 1).
Bit		4	→	UNBLANK
		1	→	Unblank RAMDAC Video Output
		0	→	Blank RAMDAC Video Output
Bit	3	2	→	Reserved (previously HAR clock select).
Bit		1	→	Reserved (previously the Fast TMS access bit).
Bit		0	→	DECrement image memory address
		1	→	Decrement image memory address after SMC.
		0	→	Increment image memory address after SMC.

0x2 (T2) Bit Plane Write Register. Write Only. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved								BPW7	BPW6	BPW5	BPW4	BPW3	BPW2	BPW1	BPW0

The Bit Plane Write register enables image memory bit planes for processor or HCM digitize writes to the image memory. When BPW7=1, bit 7 of the image memory is write enabled. When BPW7=0, bit 7 of the image memory is write disabled. When BPW6=1, bit 6 of the image memory is write enabled, etc. Bit Plane Write does not work with image memory boards with fewer than 32 DRAMs (such as the 4MB image memory board) and must have 0xFF loaded to operate properly.

0x3 (T3) TMS320 Status Register. Write Only. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved								T3-7	T3-6	T3-5	T3-4	T3-3	T3-2	T3-1	T3-0

The PC reads this register as PC0. It provides TMS320 to PC communication.

0x4 (T4) Video Address Counter Low. Write Only. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

0x5 (T5) Video Address Counter High. Write Only. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				VA27	VA26	VA25	VA24	VA23	VA22	VA21	VA20	VA19	VA18	VA17	VA16

The 28 bit video address counter provides the image memory address for video digitize or display. Writes to the counters must take place when the SMC bit of the HCM is not generating image memory cycles (when HCBL=0, VBL=0, or when the HCM is disabled). Usually, the TMS320 writes the counters once per line or once per field. The T4 counter contains the low 16 bits of the image memory address. The T5 counter contains the upper 8 bits of the image memory address. The counters address the image memory as four pixels (32 bits). HCM bits Bf1 and Bf0 provide one of four pixel selection. See the **Architecture** chapter for details.

0x6 (T6) Memory Offset Register. Write/Read. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MO15	MO14	MO13	MO12	MO11	MO10	MO9	MO8	MO7	MO6	MO5	MO4	MO3	MO2	MO1	MO0

The MO register is used by the TMS320 and the PC to access more than the first 64KB of the image memory address space. The MO register can be written and read by both the PC and the TMS320. The processor with access to the image memory also has access to the MO register. The contents of the MO register is added to bits 15 and 14 of the processor address to form the image memory address.

When the Model 12 is connected to an IMAGE MEMORY EXPANSION board, two bits of the MO are used to select one of four groups of four memory modules on the IMAGE MEMORY EXPANSION board. A carry from the lower bits of the address does not affect the module select bits. When 16MB modules are installed, MO15 and MO14 select one of four groups of four memory modules. When 4MB modules are installed, MO13 and MO12 select one of four groups of four memory modules. When 1MB modules are installed, MO11 and MO10 select one of four groups of four memory modules.

0x7 (T7) Clock Vertical Control Output Register. Read.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Valid															

A read of T7 causes the contents of the Vertical Control *Input* Register (see below) to be loaded into the Vertical Control *Output* Register. See the section on the VCR for details. Data read by the TMS320 is invalid.

0x7 (T7) Vertical Control Input Register. Write. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Res Res								HLS (HLS)	ODD (ODD)	Res	VEPI (EPI)	VSPI (SPI)	VACT (FLW)	CURV (CUR)	NREF (REF)

Bit 7 → Half Line Select
- 1 → Select HCM bit 7 (HCS) as TMS320 level 0 interrupt.
- 0 → Select HCM bit 1 (HCSEPI) as TMS320 level 0 interrupt.

Bit 6 → ODD
- 1 → Odd video field.
- 0 → Even video field.

Bit 5 → Reserved

Bit 4 3 → Vertical Equalization and Serration Pulse Interval
- 0 0 → Bit 7 (HCS) of HCM.
- 0 1 → Bit 1 (HEPI) of HCM.
- 1 0 → Bit 6 (HSPI) of HCM.
- 1 1 → Bit 7 (HCS) of HCM.

When PHS0=0, bits 4 and 3 select the HCM bit to generate the composite sync output and the sync on green video output.

Bit 2 → Vertical ACTive
- 1 → Video active and vertically unblanked (SMC to image memory allowed).
- 0 → Video blanked (TMS or PC access to image memory allowed).

Bit 1 → CURsor Vertical
- 1 → Cursor (Bt431) vertical input high.
- 0 → Cursor (Bt431) vertical input low (active).

Bit 0 → No REFresh
- 1 → Disable PC bus image memory refresh.
- 0 → Enable PC bus image memory refresh.

Allows PC bus refresh cycles to perform refresh of image memory in vertical blanking or when HCM is stopped.
Allows PC bus refresh to be stopped 1 line prior to VACT=1.

0x8 (T8) Horizontal Test. Read Only. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved															HDAT

Bit 0 → Horizontal DATa
- 1 → No change since last read.
- 0 → HTST = 1 and selected sync source = 0.

Reading T8 sets HDAT to a 1 after the TMS320C25 has read the data. The logical "AND" of HTST = 1 and incoming sync = 0 will clear HDAT. HDAT provides the TMS320C25 with the capability of measuring the number of pixels in the horizontal interval of the selected sync or video input. This bit is used with the HTST bit (bit 11) of the HCM. By setting HTST = 1 at the highest address of the HCM, testing HDAT, and decrementing the address at which HTST = 1, and iterating, the width of the horizontal interval may be determined. The width of the sync pulse may also be determined.

The T8 register was the Horizontal Address Register on Model 5 and 10.

0x9 (T9) Look Up Tables. Read/Write. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Zero on read								LUT7	LUT6	LUT5	LUT4	LUT3	LUT2	LUT1	LUT0

Data to the Brooktree Bt453 RAMDAC control registers and lookup tables.

0xA (T10) Cursor Control. Read/Write. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Zero on read								CUR7	CUR6	CUR5	CUR4	CUR3	CUR2	CUR1	CUR0

Data to the Brooktree Bt431 cursor control registers and data. Dual Bt431s are an option on the Model 12. T13 bit 2 selects the cursor to be controlled when dual Bt431s are installed.

0xB (T11) Reserved.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved															

0xC (T12) Control Register 2. Write Only. Cleared on power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved											TACC	MC3	MC2	MC1	MC0

Bit 4 → TMS320 ACcess Control
- 1 → TMS320 has Image Memory access (no PC access).
- 0 → TMS320 may access Image Memory when PC1 bit 4 → 0

See the **Image Memory** chapter for details.

Bit 3 → MC3, pin 16 of the V8 connector.
Bit 2 → MC2, pin 14 of the V8 connector.
Bit 1 → MC1, pin 12 of the V8 connector.
Bit 0 → MC0, pin 10 of the V8 connector.

MC3 thru MC0 are enabled by V8C1 and V8C0 in register T13.
MC3 thru MC0 are used for camera control functions.
MC1 and MC0 select one of four video and pixel clock inputs of the Pixel Clock and Video Four Input Multiplexer Module.

0xD (T13) Control Register 3. Write Only. Cleared on power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved								IMTS 1	IMTS 0	V8C1 V8C1	V8C0 V8C0	SYCL SYCL	CURS CURS	ELUT ELUT	IM16 IM16

Bit 7 → IMTS1
1 → Reserved.
0 → Reserved.

Bit 6 → IMTS0
1 → Reserved.
0 → Reserved.

Bit 5 → V8 Control 1 (V8C1 in table below). Controls V8 video I/O.
Bit 4 → V8 Control 0 (V8C0 in table below). Controls V8 video I/O.

V8C1	V8C0	Data	PHV	MC0-3	Analog	→Comments
1	1	In	In	Out	Off	→ Data in, V8 PHV in (do not select in display mode).
1	0	Out	Out	Out	Off	→ Data out, V8 PHV out.
0	1	Out	In	Out	Off	→ Data out to VGA adapter, V8 PHV in.
0	0	Off	Off	Off	In	→ PHV in from analog connector & module.

Bit 3 → SYnc and CLamp (when CLMP jumper is in "M" position)
1 → Programmable sync detect and clamp circuit.
0 → Sync stripper circuit and clamp.

Bit 2 → CURSor
1 → Select optional Bt431 cursor 1.
0 → Select standard Bt431 cursor 0.

Bit 1 → Enable LUT
1 → Enable A-D register output to LUT connector.
0 → Disable A-D register output to LUT connector.

Bit 0 → TMS320 Image Memory 16
1 → TMS320 16 bit image memory access.
0 → TMS320 8 bit image memory access.

0xE (T14) C40 Communication Port Data. Read/Write. Undefined at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Zero on read								CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Register T14 provides the C25 with controls for communication port 5 of the TMS320C40 on the optional COC40 board. Prior to passing data, ownership of the communication port must be established. At TMS320C40 reset (C40G0 = 0, bit 6, T13), the C40 does not have possession of the port 5 ownership token and the token is not being requested.

0xF (T15) C40 Communication Port Control. Read/Write. Cleared at power-up.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved														DRDY	DIR TRQ

Bit 1 → Data ReaDY (Read only)
1 → Data ready.
0 → Data not ready.

Bit 0 → DIRection (Read) / Transmit ReQuest (Write)
1 → (Read) Data direction is in.
0 → (Read) Data direction is out.

1 → (Write) Request token if not owner or hold token if owner.
0 → (Write) Allow release of token.

6.C Horizontal Control Memory

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HCMC	BNKB	DIG	SMC	HTST	HUB	BF1	BF0	HCS	HSPI	HQUL	HCLP	HTRG	HACT	HEPI	CURH
(RST)	(BfB)	(DIG)	(SMC)	(ONE)	(FLW)	(Bf1)	(Bf0)	(NIV)	(VSP)		(CLA)	(B03)	(HCB)	(SEP)	(CUR)
[RST]	[BfB]	[DIG]	[SMC]	(SYN)	[FLW]	[Bf1]	[Bf0]			[OKL]	[CLA]	[B03]	[HCB]	[OVR]	[CUR]

Mnemonics enclosed with (parenthesis) or [brackets] are shown by 4MIP in (master) or [genlock] mode respectively.

Bit 15 → Horizontal Control Memory Count
- 1 → Horizontal Control Memory counters count.
- 0 → Load Horizontal Control Memory counters with starting address.

Bit 14 → BaNKB
- 1 → A-D data clocked into bank B. Bank A data to image memory.
- 0 → A-D data clocked into bank A. Bank B data to image memory.

Bit 13 → DIG
- 1 → A-D data written to image memory (digitize).
- 0 → A-D data read from image memory (display).

Bit 12 → Start Memory Cycle
- 1 → Start image memory cycle. Generates RAS then CAS to image memory.
- 0 → Between image memory cycles (at least three 0's between 1's).

Bit 11 → Horizontal TeST
- 1 → Clock vertical sync and field detect circuit.
- 0 → Clock is low.

HTST goes to 1 at 1/3 horizontal and to 0 at 2/3 horizontal.

Bit 10 → Horizontal UnBlank
- 1 → Unblank RAMDAC video outputs.
- 0 → Blank RAMDAC video outputs.

Bit 9 8 → BuFfer
- 0 0 → Image memory input/output register 0
- 0 1 → Image memory input/output register 1
- 1 0 → Image memory input/output register 2
- 1 1 → Image memory input/output register 3

Bit 7 → Horizontal Composite Sync
- 1 → Composite sync output and sync on green video output high.
- 0 → Composite sync output and sync on green video output low.

Bit 6 → Horizontal Serration Pulse Interval
- 1 → Composite sync output and sync on green video output high.
- 0 → Composite sync output and sync on green video output high.

Bit 5 → Horizontal QUALifier
- 1 → Horizontal qualifier High.
- 0 → Horizontal qualifier Low.

Bit 4 → HCLamP
- 1 → Video input clamped to reference level when SYCL=1 (T13 bit 2).
- 0 → Video input not clamped when SYCL=1.

Bit 3 → Horizontal TRiGger
- 1 → High to CON5 (DIC) pin 20 and CON6 pin 39.
- 0 → Low to CON5 (DIC) pin 20 and CON6 pin 39.

Bit 2 → Horizontal ACTive
- 1 → HCM SMC generates image memory read/write cycles if VACT=1.
- 0 → HCM SMC generates image memory refresh cycles if VACT=1.

Bit 1 → Horizontal Equalization Pulse Interval
- 1 → Composite sync output and sync on green video output high.
- 0 → Composite sync output and sync on green video output high.

Bit 0 → CURsor Horizontal
- 1 → Cursor horizontal drive high.
- 0 → Cursor horizontal drive low. Reset Bt431 cursor horiz. counter.

6.D Video Output

The video output of the Model 12 consists of a set of three look up tables (LUTs) made of random access memory (RAM) and three digital to analog converters (DACs). The LUTs and DACs are in one integrated circuit, the Brooktree Bt453 RAMDAC. A *brief* description of the Bt453 follows. For a complete description refer to the data sheet from Brooktree.

The Bt453 has three internal 256 × 8 bit LUTs and three 24 bit overlay registers, allowing the display of up to 256 colors from a 16.8 million color palette. The output of each 256 × 8 bit LUT drives one DAC. The contents of the LUTs and the overlay registers are accessed by the TMS320C25 at register T9. The TMS320C25 data bus interface operates asynchronously to the video data.

Two control bits in register T1 specify whether the processor is accessing the address register, LUT RAM, or the overlay registers.

When the cursor is being displayed, the contents of overlay color 0 are displayed on the monitor and pixel information is ignored. On the Model 12, only overlay color 0 is used by the cursor circuitry.

ADS1 refers to bit 9 in the T1 register

Address Bits	Value	ADS1	Addresses
ADDR0 → ADDR1 counts modulo 3 (internal to RAMDAC)	00	x	Red Value
	01	x	Green Value
	10	x	Blue Value
ADDR2 → ADDR9 counts binary (these eight bits are available on the TMS320C25 data bus as RDAC7 → RDAC0 from register T9	0x00-0xFF	0	LUT RAM
	0x00	1	Reserved
	0x01	1	Overlay color 0
	0x02	1	Overlay color 1
	0x03	1	Overlay color 2

TABLE 6-1. Bt453 Address Register Operation

ADS0 refers to bit 8 in the T1 register.
Read and Write are 0 when active.

Read	Write	ADS0	ADDR1	ADDR0	Function
1	0	0	x	x	Write address register; RDAC0 → RDAC7 to ADDR2 → 9, 0 to ADDR0 → 1
1	0	1	0	0	Write Red value
1	0	1	0	1	Write Green value
1	0	1	1	0	Write Blue value, increment ADDR0 → 9, update table entry
0	1	0	x	x	READ address register; ADDR2 → 9 to RDAC0 → RDAC7
0	1	1	0	0	READ red value
0	1	1	0	1	READ green value
0	1	1	1	0	READ blue value, increment ADDR0 → 9
0	0	x	x	x	Illegal operation

TABLE 6-2. TMS320C25 to Bt453 Operation

Bt453 Operation

Assumption: video is not being displayed.

1. Load starting address of LUT RAM data.
   A. Select address register by writing 0 to bit 8 in T1.
   Write 0x0000 to T1.
   B. Output the starting address through T9 of the TMS320C25 on data bits RDAC0 → RDAC7.
2. Load LUT RAM data.
   A. Select LUT by writing a 1 to bit 8 and a 0 to bit 9 in T1.
   Write 0x0100 to T1.
   B. Output color data through T9 of TMS320C25. RED, GREEN, BLUE data are written in order to the RAM. After a write of blue data, the internal address to the LUT RAM is incremented.
3. Read address register.
   A. Write 0x0000 to T1.
   B. Read T9 of TMS320C25. Address bits 2 → 9 of the RAM are on TMS320C25 data bits RDAC0 → RDAC7.
4. Read LUT RAM data at current address location.
   A. Write 0x0100 to T1.
   B. Read T9 of TMS320C25. RED data is read first, then GREEN, then BLUE. Internal address to the LUT RAM is automatically incremented after the read of the blue data.
5. Load Cursor Overlay Color 0.
   A. Write 1 to bit 8 and 1 to bit 9 in T1.
   Write 0x0300 to T1.

B. Write RED, GREEN and BLUE data to T9.

6.E Hardware Cursor

The Model 12 uses a Brooktree Full Screen Cross Hair Cursor Generator (Bt431) with the Brooktree Bt453 to display a cursor on the video raster. Video rasters of up to 4096 × 4096 are supported. For a complete description of the Bt431 refer to the Brooktree data sheet.

The Bt431 cursor generator provides a 64 × 64 pixel user-definable cursor and/or a cross hair cursor. Both cursors may be displayed simultaneously with logical OR and exclusive-OR operations supported. Either cursor may be moved off the top, bottom, left, or right side of the display without wrap-around. The cursors may be positioned to one pixel resolution and may be individually enabled or disabled. The cross hair cursor may occupy a full screen or a window.

Circuit Description

The Bt431 is initialized and controlled by the TMS320C25. It is written to and read from the T10 register. Bits 9 and 8 in the T1 register select what function the TMS320C25 is performing during accesses to the Bt431.

ADS1 and ADS0 refer to bits 9 and 8 in the T1 Register

ADS1	ADS0	Function
0	0	Read/Write Address Register 0
0	1	Read/Write Address Register 1
1	0	Read/Write RAM location specified by Address Reg
1	1	Read/Write Control Register specified by Address Reg

TABLE 6-3. TMS320C25 Cursor Control Table

The two 8-bit address registers, cascaded to form a 16-bit address pointer register, are used to address the internal control registers and cursor RAM. After a read or write to the cursor RAM, the 9 least significant bits of the address pointer register are incremented. The TMS320C25 may load the address pointer register with the desired starting RAM address and burst load new cursor RAM data by writing up to 512 bytes of data. Following a read or write cycle to RAM location 0x01FF, the address pointer register resets to 0x0000.

ADS1	Addr Reg 1	Addr Reg 0	Register/ Ram Location Addressed
0	0000 0000	0000 0000	cursor RAM addrs 0x000
0	0000 0000	0000 0001	cursor RAM addrs 0x001
.	.	.	.
.	.	.	.
0	0000 0000	1111 1111	cursor RAM addrs 0x0FF
0	0000 0001	0000 0000	cursor RAM addrs 0x100
.	.	.	.
.	.	.	.
0	0000 0001	1111 1111	cursor RAM addrs 0x1FF
1	xxxx xxxx	xxxx 0000	command register
1	xxxx xxxx	xxxx 0001	cursor (x) low register
1	xxxx xxxx	xxxx 0010	cursor (x) high register
1	xxxx xxxx	xxxx 0011	cursor (y) low register
1	xxxx xxxx	xxxx 0100	cursor (y) high register
1	xxxx xxxx	xxxx 0101	window (x) low register
1	xxxx xxxx	xxxx 0110	window (x) high register
1	xxxx xxxx	xxxx 0111	window (y) low register
1	xxxx xxxx	xxxx 1000	window (y) high register
1	xxxx xxxx	xxxx 1001	window width low register
1	xxxx xxxx	xxxx 1010	window width high register
1	xxxx xxxx	xxxx 1011	window height low register
1	xxxx xxxx	xxxx 1100	window height high register

Figure 6-1. Bt431 Address Pointer Register

After a read or write to the control registers, internal address bits 0 → 8 are incremented. While accessing the control registers, the address pointer register will reset to 0x0000 only following a write cycle to location 0x01FF. The address register is not incremented when it is accessed.

Cursor Command Register

The command register is used to control various functions of the Bt431. It is accessed with the T10 register, when bit 9 of the T1 register is 1 and the address pointer register is loaded with 0x0. The command register is not initialized and may be written to or read from at any time. On startup of the software the command register should be initialized to enable the RAMDAC to display video.

T10. Cursor Control. Read/Write. Undefined at power-up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CUR7	CUR6	CUR5	CUR4	CUR3	CUR2	CUR1	CUR0

Bit 7 → Not used

Bit 6 → 64 × 64 Cursor Enable
- 1 → Enable Cursor RAM Output
- 0 → Disable Cursor RAM Output

Bit 5 → Cross Hair Cursor Enable
- 1 → Enable Cross Hair Cursor
- 0 → Disable Cross Hair Cursor

Bit 4 → Cursor Format Control
- 1 → OR Cross Hair Cursor with RAM Cursor
- 0 → XOR Cross Hair Cursor with RAM Cursor when both 64 × 64 cursor and cross hair cursor are enabled

Bit 3 2 → Multiplex Control
- 0 0 → 1:1 Multiplexing
- 0 1 → 4:1 Multiplexing
- 1 0 → 5:1 Multiplexing
- 1 1 → Reserved

Model 12 only supports 1:1 Multiplexing

Bit 1 0 → Cross Hair Cursor Thickness
- 0 0 → 1 pixel
- 0 1 → 3 pixels
- 1 0 → 5 pixels
- 1 1 → 7 pixels

Figure 6-2. Bt431 Command Register Description

64 × 64 Cursor Positioning

When the cursor RAM is being displayed, a logic 1 in the cursor RAM enables the overlay register in the Bt453, which causes pixel information from image memory to be ignored. The cursor pattern may be changed by changing the contents of the cursor RAM.

The 64 × 64 cursor is centered about the value specified by the cursor (x,y) register. The cursor (x) register specifies the location of the 31st column of the 64 × 64 RAM (assuming the rows start with 0 for the upper left pixel and increment to 63).

Note that the Bt431 expects (x) to increase going right and (y) to increase going down as seen on the video output monitor.

The cursor (x) position is relative to the first rising edge of the pixel clock following the falling edge of the CRSRHN signal of the HCM. Software must take into account the internal pipeline delays and the amount of skew between the output cursor data and external pixel data.

The cursor (y) position is relative to the first falling edge of Horizontal Drive that is two or more pixel clock cycles after the falling edge of the CRSRVN signal of the Vertical Control Register. Note that the Bt431 begins counting lines or pixels on a falling edge.

Cross Hair Cursor Positioning

The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

The window (x,y) registers, window width registers, and window height registers determine the size of the cross hair cursor window. If a full screen cursor is desired, the window (x,y) registers should contain 0x0000, and the window width and height registers should contain 0x0FFF. If a smaller window is desired, the window registers must be

loaded with the appropriate values.

Dual Cursor Positioning

Both the 64 × 64 cursor and the cross hair cursor may be enabled for display simultaneously. In the 64 × 64 pixel area of the user-definable cursor, the contents of the cursor RAM may be logically ORed or exclusive-ORed with the cross hair cursor.

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinates of the center of the 64 × 64 pixel cursor window or the intersection of the cross hair cursor. The cursor (x) value to be written is calculated as follows:

Cx= desired screen (x) position + D + H + 37

where
D = skew (in pixels) between the output cursor data and external pixel data
H = number of pixels between the first rising edge of the pixel clock following the rising edge of CRSRHN and the first active pixel.

The cursor (y) value to be written is calculated as follows:

Cy = desired screen (y) position + V - 32

where
V = number of scan lines from the first rising edge of H drive that is two or more pixel clock cycles after the falling edge of CRSRVN and the first line of active video.

7. TMS320C25

7.A Program Memory

The TMS320C25 has a 32K × 16 bit static RAMs for program memory. The contents of the program memory are unknown at power-up. A program must be loaded by the PC into program memory before the TMS320C25 is enabled.

The PC can select program memory with bit 6 in register PC1 at logic 0. The PC may access the program memory asynchronously to TMS320C25 access. The HOLD signal to the TMS320C25 becomes active when the PC has selected the program memory and a PC read or write to the program memory takes place. The TMS320C25 finishes the current instruction and places it's control lines, address lines, and data lines in a high impedance state. The TMS320C25 then activates the HOLD ACKnowledge signal. Approximately two wait states are generated on the PC bus until HOLDACK is activated. PC bus addresses and data are gated to the program memory when the HOLDACK is active. HOLD is removed at the end of the PC bus cycle.

An exception to the generation of two PC wait states is when the TMS320C25 is performing multi-cycle instructions (using the RPT or RPTK instructions). The TMS320C25 will not assert HOLDACK until the repeat counter has gone to zero. The PC should avoid accessing program memory in this case. Too many wait states on the PC bus could cause PC memory refresh cycles to be missed, causing loss of data in the PC's memory.

7.B TMS320C25 Interrupts

The TMS320C25 has three interrupts available externally. Each interrupt has a different priority level, level 0 being the highest, level 2 being the lowest. Interrupt level 0 is used by horizontal sync. Interrupt level 1 is used by the EXT IN signal on the DB25 connector (with the Analog Module). Interrupt level 2 is from the PC. Typically, the TMS320C25 can respond to an interrupt within 5 μs.

Interrupt level 0 is generated by the HCM when the Model 12 is in master sync mode and is generated by horizontal sync from a video source when in genlock mode. Typically, the horizontal sync occurs once per line during active video, allowing the TMS320C25 to count lines. Chapter 10, Section A.4 has details on how the interrupt is generated.

Interrupt level 1 is requested when a high-to-low transition occurs on the EXT IN signal. The EXT IN signal must be brought high by the device requesting the interrupt before the next interrupt can occur.

Interrupt level 2 is requested when a low-to-high transition occurs on bit 2 of the PC1 register. This allows the PC to interrupt the TMS320C25. This signal must be brought low by the PC before another interrupt can be requested.

7.C Registers

The TMS320C25 controls various functions by reading and writing I/O registers.

7.D Data Memory

The data memory space of the TMS320C25 is used by the Image Memory and the Horizontal Control Memory (HCM). Image Memory or HCM is selected with the MSL bit in the T1 register. The TMS320C25 cannot directly access the first 1K of data memory space because of 544 words of on-chip RAM.

By loading an offset into the Memory Offset Register (MOR), access to the first 1K of image memory is possible. Use of the MOR is described in the **Image Memory** chapter.

The HCM can be addressed by the TMS320C25 by using an offset address of 32K.

8. Image Memory

The 4MEG VIDEO Model 12 uses a motherboard without image memory to provide space for the data path circuits, program memory, HCM memory and logic, A-D, video amplifier and clamp, RAMDAC and cursor, TMS320C25 and program memory, and the PC bus interface.

Two types of image memory boards are available: piggyback and expansion. The piggyback image memory board mounts on the Model 12 motherboard with two connectors at the non-bracket end of the motherboard and either 2 or 4 screws. The motherboard and image memory board require a single slot in the PC. The expansion image memory board uses a second full length slot in the PC bus adjacent to the motherboard. This configuration allows the Model 12 to be configured with a range of image memory sizes and speeds.

8.A Access and Control

Input/Output registers on the motherboard buffer data from the A-D or to the RAMDAC. The PC bus, the TMS320C25, or the Horizontal Control Memory have access to image memory. Only one of these three can access image memory at a time. When video is being digitized or displayed the processors are locked out, and the HCM controls image memory. Only one processor may access the image memory when video is blanked.

8.B Refresh

Conventional dynamic random access memory (DRAM) is used in the image memory. The word "dynamic" refers to the requirement to recharge the capacitor used to store a bit in each memory cell. The DRAM is organized in a row and column address array with the number of row addresses being equal to the number of column addresses. Each row address of a DRAM must be accessed by a read, write, or refresh cycle in a specified time period to keep the capacitors in the DRAM from discharging.

For the 64MB piggyback image memory board, 4096 row addresses must be accessed every 64 milliseconds. For the 16MB or 4MB image memory board, 1024 row addresses must be accessed every 16 milliseconds. This is a rate of one row access per 15.625 microseconds.

Image memory is 32 bits, 4 pixels, or 4 bytes wide. Video access to image memory is 4 pixels wide. PC or TMS access to image memory is either 16 or 8 bits. If the access is a read cycle, all 32 bits are read. If the access is a write cycle, all 8 or 16 bits are written while the other 24 or 32 bits are read. The least significant image memory addresses are the DRAM row addresses. This means that video accesses by the HCM refreshes the DRAM rows that are being addressed. The one row access per 15.625 microseconds refresh requirement for standard DRAMs means that the minimum pixel clock period would be 4 microseconds, or 256 KHz. This assumes maximum cycles by the HCM. Optional, low power DRAMs which require 1/8th the refresh cycles that standard DRAMs require are also available. These low power DRAMs would decrease the minimum pixel clock period to 32 microseconds, or 32 KHz.

To be certain that all DRAM row addresses are refreshed, the HCM can generate refresh cycles during horizontal blanking. For RS-170 timing, 5 or more refresh cycles must be performed during horizontal blanking. Optional, low power DRAMs which require 1/8th the refresh cycles that standard DRAMs require are also available.

8.C PC Access

If video is active, the PC must wait for vertical blanking before accessing the image memory. Accessing image memory during active video will result in invalid data being read or written, and image data may be corrupted. Video display can be stopped to give the PC full access to image memory. No PC bus wait states are used during PC image memory access.

8.C.1 Processor Arbitration

Prior to accessing the image memory, the PC must verify that the TMS320C25 is not accessing image memory. The PC selects image memory with bit 6 in register PC1. A logic 1 selects image memory. PC1 bit 4 (PCIMACK) must also be logic 1. Bit 4 is an arbitration bit gated with bit 4 of the T12 register (TIMACK). The table below shows the function selected by the combinations of the arbitration bits from the PC and the TMS320C25. There is no error flag or other explicit signal to tell the PC if the TMS320C25 has access.

PCIMACK	TIMACK	Access Granted To:
0	0	TMS320C25
0	1	TMS320C25
1	0	PC
1	1	TMS320C25

TABLE 8-1. Processor Arbitration To Image Memory

8.C.2 Memory Offset Register

To access up to 64MB of memory through a 64KB page, a 16 bit Memory Offset Register (MOR) is used. The MOR allows sliding a 16KB address "window" across the image memory by adding bits bits 14 and 15 of the processor address to the value contained in the MOR. The MOR is written by the processor (TMS320C25 or PC) with access to the image memory.

8.C.3 PC Refresh

When the PC has access to the image memory, DRAM refresh is performed during blanking using the PC bus refresh signal. PC bus refresh cycles are gated to the image memory when the Vertical Refresh Enable bit in the VCR is active. When the PC selects program memory, the image memory will still be refreshed. The image memory may also be refreshed in the horizontal blanking interval by the HCM when the PC has access to image memory and video is active.

8.D TMS320C25 Access

The TMS320C25 can access the image memory when the video is not active. The processor must set TIMACK to a 1 or both TIMACK and PCIMACK must be 0. See Table 8-1 above. The TMS320C25 selects image memory with bit 15 set to a 1 in the T1 register (0 selects the HCM). The BPW must be written with the desired bit plane mask. The MOR is used to generate addresses above 64K.

8.D.1 TMS320C25 Data Path

When 8 bit image memory access is selected by bit 0 of T13, image memory data is read on the low byte of the TMS320C25 data bus. The upper byte is a logical 0 during reads. One TMS320C25 wait state is used on image memory cycles resulting in a 160 ns cycle time.

8.D.2 TMS320C25 Addressing

When the TMS320C25 addresses image memory in 8 bit mode, the two least significant processor address bits select data from 1 of 4 banks of DRAMs. In 16 bit mode, address bit 1 selects either banks 1 and 2 or 3 and 4 of the 4 banks of DRAMs. Address bits 2 through 13 drive the image memory address lines. Address bits 14 and 15 are summed with the contents of the 16 bit Memory Offset Register. The 28 bit address is formed by the 14 lower bits of the processor address bus and the 2 upper bits of the processor address bus added to the 16 bits of the MOR. See Figure 8-1.

8.D.3 TMS320C25 Refresh

When the TMS320C25 has access to image memory, it must perform read cycles to refresh the memory when the HCM is not performing refresh. PC bus refresh cycles or HCM refresh cycles use a counter internal to the DRAM to generate the necessary refresh addresses. When the TMS is generating refresh cycles, it must generate the correct addresses to perform refresh.

For the 64MB image memory board, 4096 addresses must be accessed every 64 ms. For the 16MB or 4MB image memory board, 1024 addresses must be accessed every 16 ms. Image memory is refreshed by the TMS320C25 when it reads (or writes) addresses greater than modulo 4 (0, 4, 8, 12, etc.). For example, accessing address 0 accesses and refreshes four banks of DRAMs. If addresses 1 thru 3 are accessed, the same row in all four DRAM banks is again accessed and refreshed. When address 4 is accessed a new row in all four DRAM banks is accessed and refreshed.

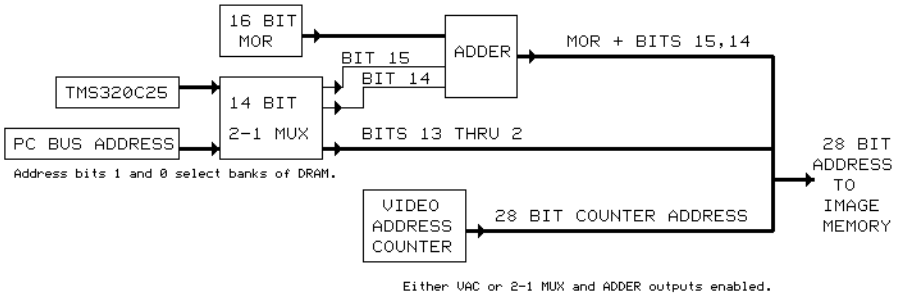

Figure 8-1. Image Memory Address Path

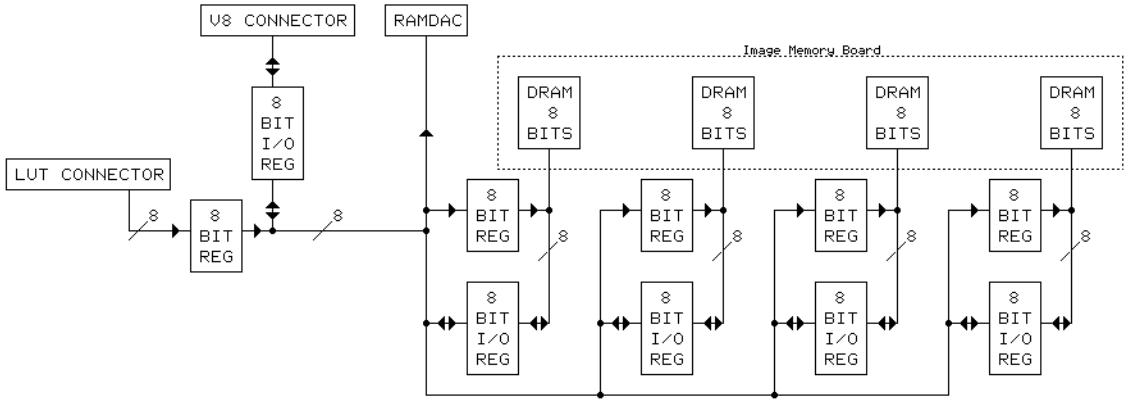

Figure 8-2. Image Memory Video Data Path

8.E Digitize

The output of the A-D (thru the LUT connector and register) or the V8 input data is routed to one of the 4 input registers or the 4 input/output registers. The 4 input registers and 4 input/output registers are used as alternate pairs. While one register at a time of the input registers are loaded, the outputs from the 4 input/output registers are enabled and their data is written to the image memory. After the 4 input registers are loaded, their outputs are enabled and their data is written to the image memory, while the input/output registers are loaded with 4 more pixels. The data is loaded into each register sequentially under control of the HCM. The LUT connector register input or the V8 connector input connects to the RAMDAC which allows the input to be displayed. The video output may be blanked while digitizing by writing a 0 to the BLACKN bit in the T1 register.

The Bit Plane Write (BPW) register can be used to prevent writing individual bit planes. The BPW does not affect display operations. BPW is not available on: image memory boards with fewer than 32 DRAMs, the IMAGE MEMORY EXPANSION, the COC40, or the COC402.

8.F Display

To generate a video display, an image memory read operation is initiated by the HCM. The 32 bits from the image memory are read and loaded into the 4 eight bit I/O registers simultaneously. The output of one 8 bit I/O register is enabled to drive the RAMDAC. At each of the next three pixel clocks the outputs of the other three I/O registers are enabled to the RAMDAC. After the contents of the fourth I/O register is loaded into the RAMDAC, and before the contents of the first I/O register are to be loaded into the RAMDAC, image memory data from the next image memory address is loaded into the 4 I/O registers and the cycle repeats.

During digitize and display the Horizontal Control Memory (HCM) controls the image memory. The HCM generates the Row Address Strobe (RAS), Column Address Strobe (CAS), Write, output enable, and signals to control data paths. The Video Address Counter (VAC) generates image memory addresses and is incremented at the end of each HCM generated RAS. The TMS320C25 loads the VAC during horizontal blanking. Digitized video data can be stored sequentially, from left to right and top to bottom, in raster scan order. Video data can also be stored from bottom to top and/or right to left. Loading the VAC during active video will cause unpredictable results. The VAC is not reset during vertical or horizontal blanking times. If a new address is not loaded by the TMS320C25, the VAC

will continue from the previous line.

To determine the starting address of each line of video during digitize or display, the following algorithm can be used.

Let:
P = the total number of active pixels per line
L = the total number of lines per image
B= the current buffer
N= the line number

The starting address is:

$$(P/4)\times N \quad (1)$$

if B = 0, and is:

$$(P/4)\times(L+N)\times B \quad (2)$$

if B>0.

For example, let:

P = 512
L = 3
N = 2
B = 0

From equation (1) above, the starting address of the third line is calculated as:

$$(512/4)\times 2=256$$

Let:
P = 512
L = 3
N = 2
B = 1

From equation (2) above, the starting address of the third line in the second buffer is calculated as:

$$(512/4)\times(3+2)\times 1=640$$

Buffer 0 Pixel Addresses

0	Line 0	127
128	Line 1	255
256	Line 2	383

Buffer 1 Pixel Addresses

384	Line 0	511
512	Line 1	639
640	Line 2	767

8.G Memory Offset Register

A 16 bit Memory Offset Register (MOR) and adder allow the PC and TMS320C25 to access up to 1GB of image memory. The PC loads the register only when it has access to the image memory; the TMS320C25 loads the register only when it has access to the image memory. Address bits 15 and 14 of the processor accessing image memory are added to the contents of the MOR. The low bit of the adder becomes bit 14 of the address to the image memory.

The adder outputs and the 2-1 processor address mux outputs are enabled to the image memory when video is blanked. The outputs of either the VAC, or the adder and 2-1 address mux, are enabled to the image memory board.

Incrementing the MOR contents by one increments the image memory address by 16K. The MOR is accessed by the TMS320C25 as register T6. The PC accesses the MOR as registers PC2 and PC3.

8.H Bit Plane Write

The Bit Plane Write (BPW) register allows one or several of the 8 bit planes of the image memory to be written. The BPW is active when the PC, HCM, or TMS320C25 are writing image memory, and is useful when writing image memory data over text or graphics. The BPW register is accessible only by the TMS320C25 as register T2. Bit zero of the BPW register write enables or disables bit plane zero of the image memory. Bit one write enables or disables bit plane one, etc. A 0 in a bit position disables writes to the respective bit plane. A 1 in a bit position enables writes to the respective bit plane. Read or refresh operations are not affected. BPW is not available on: image memory boards with fewer than 32 DRAMs, the IMAGE MEMORY EXPANSION, the COC40, or the COC402.

9. Horizontal Control Memory

The Horizontal Control Memory (HCM) is used to generate video timing information, and to control the video data path and image memory during digitize and display operations. The HCM can also refresh image memory during horizontal blanking.

The HCM is an 8K × 16 bit fast static RAM (optional 32K). The TMS320C25 writes and reads the HCM. The TMS320C25 selects HCM access with bit 15 in the T1 register. The TMS320C25 must begin addressing the HCM at 32K (0x80000), because addresses from 0 to 1023 access data RAM in the TMS320C25. By starting at address 32K (0x8000), the low 14 bits are zeros, and address 0 is seen at the HCM.

When video is being displayed or digitized, the HCM address is generated by the HCM address counter. The address counter is started and stopped by the TMS320C25. The rising or falling edge of horizontal sync causes the counter to load the HCM starting address. The starting address is selected by the TMS320C25, as shown in Table 9-1. HS16K, HS4K, and HS1K are bits 7, 6, and 13, respectively, of the T1 register.

For example, when used to generate RS-170 timing, which has 910 pixels per line (14.318 MHz pixel clock), an HCM sequence to digitize video is stored in the first 1024 words and a sequence to display video is stored in the next 1024 words. To change from digitize to display or from display to digitize, the starting address of the HCM is selected with the T1 register. The change occurs at the next horizontal sync.

An alternative method of switching from digitize to display is to rewrite the HCM when video is blanked. This method is necessary if one or both of the HCM sequences takes up the entire HCM. When generating or genlocking to video with timing other than RS-170, the length of the line, in pixel clocks, determines the minimum size of the HCM block needed. For example, if an 8K HCM is installed and a line with greater than 7K pixels is being digitized and RS-170 is being displayed, the RS-170 sequence would have to be written in the low 1K address. With the same video formats being used, but a 32K HCM installed, the digitize sequence could be stored in the block beginning at 1K and the display sequence stored in the block beginning at 0. Changing HS1K from 1 to 0 would switch modes.

HS16K	HS4K	HS1K	Starting address	
0	0	0	0	0x0000
0	0	1	1024	0x0400
0	1	0	4096	0x1000
0	1	1	5120	0x1400
1	0	0	16384	0x4000
1	0	1	17408	0x4400
1	1	0	20480	0x5000
1	1	1	21504	0x5400

TABLE 9-1. Horizontal Control Memory Starting Addresses

9.A HCM Bit Description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HCMC (RST) [RST]	BNKB (BfB) [BfB]	DIG (DIG) [DIG]	SMC (SMC) [SMC]	HTST (ONE) (SYN)	HUB (FLW) [FLW]	BF1 (Bf1) [Bf1]	BF0 (Bf0) [Bf0]	HCS (NIV)	HSPI (VSP)	HQUL [OKL]	HCLP (CLA) [CLA]	HTRG (B03) [B03]	HACT (HCB) [HCB]	HEPI (SEP) [OVR]	CURH (CUR) [CUR]

Mnumonics enclosed with (parenthesis) or [brackets] are shown by 4MIP in (master) or [genlock] mode respectively.

Bit 15 → Horizontal Control Memory Count
- 1 → Horizontal Control Memory counters Count.
- 0 → Load Horizontal Control Memory counters with starting address.

Bit 14 → BaNKB
- 1 → A-D data clocked into bank B. Bank A data to image memory.
- 0 → A-D data clocked into bank A. Bank B data to image memory.

Bit 13 → DIG
- 1 → A-D data written to image memory (digitize).
- 0 → A-D data read from image memory (display).

Bit 12 → Start Memory Cycle
- 1 → Start image memory cycle. Generates RAS then CAS to image memory.
- 0 → Between image memory cycles (at least three 0's between 1's).

Bit 11 → Horizontal TeST
- 1 → Clock vertical sync and field detect circuit.
- 0 → Clock is low.

HTST goes to 1 at 1/3 horizontal and to 0 at 2/3 horizontal.

Bit 10 → Horizontal UnBlank
- 1 → Unblank RAMDAC video outputs.
- 0 → Blank RAMDAC video outputs.

Bit 9 8 → BuFfer
- 0 0 → Image memory input/output register 0
- 0 1 → Image memory input/output register 1
- 1 0 → Image memory input/output register 2
- 1 1 → Image memory input/output register 3

Bit 7 → Horizontal Composite Sync
- 1 → Composite sync output and sync on green video output high.
- 0 → Composite sync output and sync on green video output low.

Bit 6 → Horizontal Serration Pulse Interval
- 1 → Composite sync output and sync on green video output high.
- 0 → Composite sync output and sync on green video output high.

Bit 5 → Horizontal QUALifier
- 1 → Horizontal QUALifier High.
- 0 → Horizontal QUALifier Low.

Bit 4 → HCLamP
- 1 → Video input clamped to reference level when SYCL=1 (T13 bit 2).
- 0 → Video input not clamped when SYCL=1.

Bit 3 → Horizontal TRiGger
- 1 → High to CON5 (DIC) pin 20 and CON6 pin 39.
- 0 → Low to CON5 (DIC) pin 20 and CON6 pin 39.

Bit 2 → Horizontal ACTive
- 1 → HCM SMC generates image memory read/write cycles if VACT=1.
- 0 → HCM SMC generates image memory refresh cycles if VACT=1.

Bit 1 → Horizontal Equalization Pulse Interval
- 1 → Composite sync output and sync on green video output high.
- 0 → Composite sync output and sync on green video output high.

Bit 0 → CURsor Horizontal
- 1 → CURsor Horizontal drive high.
- 0 → CURsor Horizontal drive low. Reset Bt431 cursor horiz. counter.

HCMC is used in master sync mode to set the HCM counters to a starting value, determined by HS16K, HS4K, and HS1K in the T1 register.

DIG selects whether the image memory is being written to or read from.

SMC is used to clock the image memory address counters and cause image memory read/write and refresh cycles.

Read/write cycles occur when SMC is high and HACT is low. The counters are incremented or decremented at the high-to-low transition of SMC, when HACT is low.

SMC is also used to generate refresh cycles during horizontal blanking. Image memory refresh cycles occur when SMC is high and HACT is high. The image memory address counters are not incremented in this case.

HUB blanks the video output.

BF1 and *BF0* select the image memory I/O register that video data is read from or written to.

HCS generates the horizontal sync signal during active video.

HSPI generates the vertical serration pulses in the vertical sync interval.

HQUL may be used to filter noisy composite sync signals.

HTRG may be used to signal a device connected to the Digital Interface Connector's pin 20.

HACT is used to enable digitize, display, and refresh operations.

HEPI generates the equalizing pulses during the vertical sync interval.

CURH provides a "horizontal" signal to the Bt431 cursor generator.

9.B Operation of the Horizontal Control Memory

To start the HCM counters at zero, and clock the HCM registers, the TMS320C25 writes 0x1800 to T1. Referring to the T1 register description, HS1K starts the HCM counter at zero, HCMEN enables the HCM counter, and HCMCLR enables the outputs of the HCM registers.

To start the HCM counters at 1024, and enable the HCM registers, load 0x3800 into T1. Bit 13 selects starting count 1024, HCMEN enables the HCM counter, and HCMCLR enables the HCM register outputs.

The HCM counters and registers are clocked with the pixel clock. The count increments only when the HCM is enabled, with HCMEN. The registers are clocked continuously. The outputs of the registers may be cleared with HCMCLR low. HCMCLR has no effect on the operation of the counters. The first rising edge of the pixel clock after the load to the HCM causes the counters to load the starting address selected by HS16K, HS4K, and HS1K.

9.B.1 Horizontal Control Memory Counter Load

The TMS320C25 can cause a load by making HCMEN in the T1 register zero. This should only be done when video is blanked, or loss of image data will result.

During digitize or display, PHS1 and PHS0 (in the T1 register) select 1 of 4 combinations of load sources and pixel clock sources. Table 9-2 shows the 4 load source selections and the operating mode.

PHS1	PHS0	Load Source Selection	Mode
0	0	Load HCM on HCMC	Master 1
0	1	Load HCM on Composite Sync Input	Genlock 1
1	0	Load HCM on HCMC	Master 2
1	1	Load HCM on External H Sync Input	Genlock 2

TABLE 9-2. HCM Load Source Selections

When PHS1 = PHS0 = 0 (Master Mode 1), the HCM loads itself, using the HCMC bit. In this mode the Model 12 is generating video timing signals that peripheral devices may use for synchronization.

When PHS1 = 0 and PHS0 = 1 the Model 12 is in Genlock Mode 1. The Model 12 will synchronize itself to the sync source. The HCM is loaded on the leading or trailing edge of input composite sync. The edge is selected with HCTS in the T1 register. HCTS high will cause a load at the leading edge of composite sync. The load is 1 pixel clock cycle in duration.

When PHS1 = 1 the HCM may be loaded with either HCMC, (from the HCM), or H Sync from the DDI/DIC (depending on the state of PHS0). When PHS0 = 0 HCMC is used, and Master Mode 2 is selected. The difference from Master Mode 1 is the source of the pixel clock. This is discussed in the **Pixel Clock Select** section below.

When PHS1 = 1 and PHS0 = 1 Genlock Mode 2 is selected. In this mode the load is from the V8 or DB25 thru the Analog Module. The load of the HCM counter will last as long as H Sync is low. This mode also uses the pixel clock signal on the V8 or from the DB25 thru the Analog Module.

The programming of the HCM is dependent upon the loading method used. In Master Modes 1 and 2, when the HCM loads itself, the load lasts for 1 pixel clock. In Genlock Mode 1, the load lasts for 1 pixel clock also. In Genlock Mode 2, the load will last *as long as horizontal sync is low*. In RS-170, this is about 5 μs (with a 14.318 MHz pixel clock, 71 pixel clocks). In Master Mode 1 or 2, after a load, there will be roughly 10 μs before active video. In genlock mode using the external pixel clock, there may be only 2 to 5 μs.

Genlock Mode 2 is selected when the camera pixel clock is used. When setting parameters in 4MIP, the fact that HCM load lasts for about 5 μs, and pixel zero is at the end of sync, must be taken into account. (In Genlock Mode 1 pixel zero is at the beginning of sync, and load lasts for one pixel clock cycle). By using the *Video Format for RS-170 with Video Tape Recorder*, the HCM parameters will be set for proper operation in this mode.

9.B.2 Pixel Clock Select

PHS1	PHS0	Pixel Clock	Mode
0	0	JP6	Master 1
0	1	PCGM	Genlock 1
1	0	Data Clk	Master 2
1	1	Data Clk	Genlock 2

TABLE 9-3. Pixel Clock Select

In Master Mode 1, the pixel clock may be selected with the PCLK jumper to be either the PC Bus clock (14.318 MHz), the Pixel Clock Generator Module (frequencies from 2 MHz to 50 MHz available), or the pixel clock input from the V8 connector or the DB25 connector thru the Analog Module. When the Pixel Clock Generator Module (PCGM) is selected in this mode it is free running.

In Genlock Mode 1, the PCGM is used as the pixel clock. The PCGM is synchronized with the input sync signal. The synchronization can occur at the high-to-low transition of sync or the low-to-high transition of sync. The HCM

counter is loaded on the same transition.

Master Mode 2 uses the pixel clock input from the V8 connector or the DB25 connector thru the Analog Module.

Genlock Mode 2 uses the pixel clock input as in Master Mode 2. The difference from Genlock Mode 1 is that the HCM counter is loaded by the input H Sync.

9.C Programming the Horizontal Control Memory

The HCM has three functions. The first is to control the image memory during digitize and display of video. The second is to generate horizontal video timing signals. The third is to perform image memory refresh during horizontal blanking. It performs these functions by operating as a microsequencer. A "program" or "sequence" is loaded into the HCM by the TMS320C25. This program may be generated by either the PC or the TMS320C25. Once the program is loaded, the TMS320C25 can enable the HCM by enabling the HCM address counter. The counter is incremented by the pixel clock, thus for each clock cycle a new "instruction" is output from the HCM. The instruction is then used by other logic on the Model 12.

The program for horizontal video timing depends on whether the Model 12 will be generating video timing (master mode) or synchronized with a source of video timing (genlock mode).

The following information is needed to program the HCM to digitize, display, and generate video timing:

The number of pixels per line.
The number of pixels per line that are blanked.
The number of pixels per line that are to be digitized.
The number of pixels per line that are to be displayed.
The width in pixels of equalization pulses (if present).
The width in pixels of serration pulses (if present).
The width in pixels of horizontal sync pulses.
The number of pixels from the end of horizontal sync to the first active pixel.

More information on horizontal sync pulses, equalizing pulses and serration pulses is given in the **RS-170 Video Timing Generation** chapter.

The number of blanked pixels refers to horizontal blanking, and is not necessarily the same as the difference between the number of pixels per line and the number of pixels that are digitized (or displayed).

9.D HCM Refresh Timing and Rules

```
   HORIZONTAL ACTIVE VIDEO SMC CONTROLLED REFRESH

SMC=0 for three pixels prior to first SMC.
HCB=0 and DIG=0 one pixel prior to first SMC.
HCB=0 and DIG=0 until four pixels after the last SMC.
SMC is spaced no closer than every fourth pixel.

xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx     xxx xxx RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx     xxx xxx RST
        xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
        xxx xxx xxx xxx xxx xxx xxx xxx xxx SMC     xxx RST first refresh cycle
        xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
        xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
        xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
        xxx xxx xxx xxx xxx xxx xxx xxx xxx SMC     xxx RST typical refresh cycle
        xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
        xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
        xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
```

```
       xxx xxx xxx xxx xxx xxx xxx xxx xxx SMC     xxx RST last refresh cycle
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
       xxx xxx xxx xxx xxx xxx xxx xxx xxx     xxx xxx RST
   HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx     xxx xxx RST  "xxx" = don't care
```

9.E HCM Digitize Timing and Rules - Pixel Width of 1

```
   HCM DIGITIZE RULES

HCB=1 at first DIG.
HCB=0 after the last DIG.
SMC is spaced no closer than every fourth pixel.
FLW=1 at first DIG.
FLW=0 after last (Bf0,Bf1)=(1,1).
B14=0 at first DIG.
B14 toggles on (Bf0,Bf1)=(1,1) to (Bf0,Bf1)=(0,0) transition.
SMC leads (Bf0,Bf1)=(1,1) to (Bf0,Bf1)=(0,0) transition by 1 pixel.
DIG=1 for four pixels after last SMC.
HCLP=1 from 0 to 13% of horizontal width (based on 0 at falling edge of sync).

      LEFT TO RIGHT DIGITIZATION
      Pixel width of 1.
      Start digitize timing:

   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
       xxx xxx xxx xxx xxx xxx xxx xxx xxx SMC     xxx RST last refresh cycle
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx xxx first pixel digitized by A-D converter
       xxx xxx xxx xxx xxx xxx xxx xxx xxx         xxx RST  "xxx" = don't care
   HCB         OKL                 FLW ONE     DIG     RST
   HCB         OKL         Bf0     FLW ONE     DIG     RST first pixel clocked into image memory register
   HCB         OKL             Bf1 FLW ONE     DIG     RST
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST first pixel displayed by D-A converter
   HCB         OKL                 FLW ONE     DIG B14 RST
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST
   HCB         OKL                 FLW ONE     DIG     RST
   HCB         OKL         Bf0     FLW ONE     DIG     RST
   HCB         OKL             Bf1 FLW ONE     DIG     RST
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST
   HCB         OKL                 FLW ONE     DIG B14 RST

End digitize timing, if the last pixel had B14=0:
   HCB         OKL                 FLW ONE     DIG     RST
   HCB         OKL         Bf0     FLW ONE     DIG     RST
   HCB         OKL             Bf1 FLW ONE     DIG     RST
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST
   HCB         OKL                     ONE     DIG B14 RST last pixel clocked into image memory register
   HCB         OKL                     ONE     DIG B14 RST
   HCB         OKL                     ONE     DIG B14 RST last pixel displayed by D-A converter
   HCB         OKL                     ONE     DIG B14 RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx

End digitize timing, if the last pixel had B14=1:
   HCB         OKL                 FLW ONE     DIG B14 RST
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST last pixel clocked into image memory register
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.F HCM Digitize Timing - Pixel Width of 2

```
        Pixel width of 2.
     Start digitize timing:
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx first pixel digitized by A-D converter
   HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST  "xxx" = don't care
   HCB         OKL                 FLW ONE     DIG     RST
   HCB         OKL                 FLW ONE     DIG     RST first pixel clocked into image memory register
   HCB         OKL         Bf0     FLW ONE     DIG     RST first pixel clocked into image memory register
   HCB         OKL         Bf0     FLW ONE     DIG     RST second pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST second pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST  third pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  third pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST   fourth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST   fourth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST    eighth pixel
   HCB         OKL                 FLW ONE     DIG     RST    eighth pixel
   HCB         OKL                 FLW ONE     DIG     RST ninth pixel


End digitize timing, if the last pixel had B14=0:

   HCB         OKL                 FLW ONE     DIG     RST last-4 pixel
   HCB         OKL                 FLW ONE     DIG     RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST last pixel
   HCB         OKL                     ONE     DIG B14 RST last pixel
   HCB         OKL                     ONE     DIG B14 RST
   HCB         OKL                     ONE     DIG B14 RST
   HCB         OKL                     ONE     DIG B14 RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
End digitize timing, if the last pixel had B14=1:

   HCB         OKL                 FLW ONE     DIG B14 RST last-4 pixel
   HCB         OKL                 FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST last pixel
   HCB         OKL                     ONE     DIG     RST last pixel
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.G HCM Digitize Timing - Pixel Width of 3

```
        Pixel width of 3.
     Start digitize timing:
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx first pixel digitized by A-D converter
   HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST  "xxx" = don't care
   HCB         OKL                 FLW ONE     DIG     RST
   HCB         OKL                 FLW ONE     DIG     RST first pixel
   HCB         OKL                 FLW ONE     DIG     RST first pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST first pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  second pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  second pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST  second pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST   third pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST   third pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST   third pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST    fourth pixel
```

```
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST    fourth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST    fourth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST    eighth pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST    eighth pixel
   HCB         OKL                 FLW ONE     DIG     RST    eighth pixel
   HCB         OKL                 FLW ONE     DIG     RST ninth pixel
   HCB         OKL                 FLW ONE     DIG     RST ninth pixel


End digitize timing, if the last pixel had B14=0:

   HCB         OKL                 FLW ONE     DIG     RST  last-4 pixel
   HCB         OKL                 FLW ONE     DIG     RST  last-3 pixel
   HCB         OKL                 FLW ONE     DIG     RST  last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  last-2 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST  last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST  last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  last pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST  last pixel
   HCB         OKL                     ONE     DIG B14 RST  last pixel
   HCB         OKL                     ONE     DIG B14 RST
   HCB         OKL                     ONE     DIG B14 RST
   HCB         OKL                     ONE     DIG B14 RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
End digitize timing, if the last pixel had B14=1:

   HCB         OKL                 FLW ONE     DIG B14 RST last-4 pixel
   HCB         OKL                 FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL                 FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST last pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST last pixel
   HCB         OKL                     ONE     DIG     RST last pixel
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.H HCM Digitize Timing - Pixel Width of 4

```
        Pixel width of 4.
     Start digitize timing:
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx first pixel digitized by A-D converter
   HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST  "xxx" = don't care
   HCB         OKL                 FLW ONE     DIG     RST
   HCB         OKL                 FLW ONE     DIG     RST first pixel
   HCB         OKL                 FLW ONE     DIG     RST first pixel
   HCB         OKL                 FLW ONE     DIG     RST first pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST first pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  second pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  second pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST  second pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST  second pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST   third pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST   third pixel
```

```
   HCB         OKL             Bf1 FLW ONE     DIG     RST   third pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST   third pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST    fourth pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST    fourth pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST    fourth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST    fourth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL                 FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST fifth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST  sixth pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST   seventh pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST    eighth pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST    eighth pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST    eighth pixel
   HCB         OKL                 FLW ONE     DIG     RST    eighth pixel
   HCB         OKL                 FLW ONE     DIG     RST ninth pixel
   HCB         OKL                 FLW ONE     DIG     RST ninth pixel
   HCB         OKL                 FLW ONE     DIG     RST ninth pixel


End digitize timing, if the last pixel had B14=0:

   HCB         OKL                 FLW ONE     DIG     RST last-4 pixel
   HCB         OKL                 FLW ONE     DIG     RST last-3 pixel
   HCB         OKL                 FLW ONE     DIG     RST last-3 pixel
   HCB         OKL                 FLW ONE     DIG     RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST last-2 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST last-2 pixel
   HCB         OKL         Bf0     FLW ONE     DIG     RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST last-1 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST last-1 pixel
   HCB         OKL             Bf1 FLW ONE     DIG     RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST last pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST last pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG     RST last pixel
   HCB         OKL                     ONE     DIG B14 RST last pixel
   HCB         OKL                     ONE     DIG B14 RST
   HCB         OKL                     ONE     DIG B14 RST
   HCB         OKL                     ONE     DIG B14 RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
End digitize timing, if the last pixel had B14=1:

   HCB         OKL                 FLW ONE     DIG B14 RST last-4 pixel
   HCB         OKL                 FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL                 FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL                 FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-3 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL         Bf0     FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-2 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL             Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST last-1 pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST last pixel
   HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST last pixel
   HCB         OKL         Bf0 Bf1 FLW ONE SMC DIG B14 RST last pixel
   HCB         OKL                     ONE     DIG     RST last pixel
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   HCB         OKL                     ONE     DIG     RST
   xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.I HCM Digitize Timing - Right to Left Digization - Pixel Width of 1

```
      RIGHT TO LEFT DIGITIZATION
   Pixel width of 1.
   Start digitize timing:
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx first pixel digitized by A-D converter
HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST  "xxx" = don't care
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE SMC DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE SMC DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE SMC DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST

   RIGHT TO LEFT DIGITIZATION
   Pixel width of 1.
End digitize timing, if the last pixel had B14=0:
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE SMC DIG     RST
HCB         OKL                     ONE     DIG B14 RST last pixel
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
   RIGHT TO LEFT DIGITIZATION
   Pixel width of 1.
End digitize timing, if the last pixel had B14=1:
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE SMC DIG B14 RST
HCB         OKL                     ONE     DIG     RST last pixel
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.J HCM Digitize Timing - Right to Left Digization - Pixel Width of 2

```
      RIGHT TO LEFT DIGITIZATION
   Pixel width of 2.
   Start digitize timing:
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx first pixel digitized by A-D converter
HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST  "xxx" = don't care
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL             Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE SMC DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL             Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE SMC DIG B14 RST

   RIGHT TO LEFT DIGITIZATION
   Pixel width of 2.
End digitize timing, if the last pixel had B14=0:
```

```
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE SMC DIG     RST last pixel
HCB         OKL                     ONE     DIG B14 RST last pixel
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
   RIGHT TO LEFT DIGITIZATION
   Pixel width of 2.
End digitize timing, if the last pixel had B14=1:
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE SMC DIG B14 RST last pixel
HCB         OKL                     ONE     DIG     RST last pixel
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.K HCM Digitize Timing - Right to Left Digization - Pixel Width of 3

```
      RIGHT TO LEFT DIGITIZATION
   Pixel width of 3.
   Start digitize timing:
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx first pixel digitized by A-D converter
HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST  "xxx" = don't care
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL             Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE SMC DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL             Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE SMC DIG B14 RST

   RIGHT TO LEFT DIGITIZATION
   Pixel width of 3.
End digitize timing, if the last pixel had B14=0:
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
```

```
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST last pixel
HCB         OKL                 FLW ONE SMC DIG     RST last pixel
HCB         OKL                     ONE     DIG B14 RST last pixel
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
   RIGHT TO LEFT DIGITIZATION
   Pixel width of 3.
End digitize timing, if the last pixel had B14=1:
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST last pixel
HCB         OKL                 FLW ONE SMC DIG B14 RST last pixel
HCB         OKL                     ONE     DIG     RST last pixel
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.L HCM Digitize Timing - Right to Left Digization - Pixel Width of 4

```
      RIGHT TO LEFT DIGITIZATION
   Pixel width of 4.
   Start digitize timing:
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx first pixel digitized by A-D converter
HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST  "xxx" = don't care
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL             Bf1 FLW ONE     DIG     RST  first pixel
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE SMC DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL             Bf1 FLW ONE     DIG B14 RST  fifth pixel
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE SMC DIG B14 RST

   RIGHT TO LEFT DIGITIZATION
   Pixel width of 4.
End digitize timing, if the last pixel had B14=0:
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
```

```
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL             Bf1 FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL         Bf0     FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST
HCB         OKL                 FLW ONE     DIG     RST last pixel
HCB         OKL                 FLW ONE     DIG     RST last pixel
HCB         OKL                 FLW ONE SMC DIG     RST last pixel
HCB         OKL                     ONE     DIG B14 RST last pixel
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
HCB         OKL                     ONE     DIG B14 RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
   RIGHT TO LEFT DIGITIZATION
   Pixel width of 4.
End digitize timing, if the last pixel had B14=1:
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0 Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL             Bf1 FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL         Bf0     FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST
HCB         OKL                 FLW ONE     DIG B14 RST last pixel
HCB         OKL                 FLW ONE     DIG B14 RST last pixel
HCB         OKL                 FLW ONE SMC DIG B14 RST last pixel
HCB         OKL                     ONE     DIG     RST last pixel
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
HCB         OKL                     ONE     DIG     RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
```

9.M HCM Display Timing

This section describes the timing of HCM signals so that an image may be displayed. It does not discuss how to digitize video, refresh the image memory, or generate horizontal video timing. The example given is brief; a typical display format will require expansion of the diagram.

```
HCB=1 one pixel prior to first SMC.
HCB=0 after the last FLW.
SMC is spaced no closer than every fourth pixel.
FLW=1 at second SMC.
FLW=0 after last (Bf0,Bf1)=(1,1).
SMC leads (Bf0,Bf1)=(1,1) to (Bf0,Bf1)=(0,0) by 4 pixels, except for last (Bf0,Bf1)=(0,0).
(Bf0,Bf1)=(0,0) when SMC=1 except first and last.
Bf0=1 one pixel prior to first SMC.

Start of display timing.
Left to right display.
Pixel width of 1.
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx
xxx xxx HCB xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx RST
CUR OVR HCB                 XX7 xxx xxx     ONE SMC         RST
CUR OVR HCB                 XX7 xxx xxx     ONE             RST
CUR OVR HCB                 XX7 xxx xxx     ONE             RST
CUR OVR HCB                 XX7 Bf0 xxx     ONE             RST
CUR OVR HCB                 XX7         FLW ONE SMC         RST
CUR OVR HCB                 XX7 Bf0     FLW ONE             RST first pixel out of image memory registers
```

```
CUR OVR HCB                XX7     Bf1 FLW ONE            RST
CUR OVR HCB                XX7 Bf0 Bf1 FLW ONE            RST first pixel out of D-A
CUR OVR HCB                XX7         FLW ONE SMC        RST
CUR OVR HCB                XX7 Bf0     FLW ONE            RST
CUR OVR HCB                XX7     Bf1 FLW ONE            RST
CUR OVR HCB                XX7 Bf0 Bf1 FLW ONE            RST
CUR OVR HCB                XX7         FLW ONE            RST

End of display timing.
Left to right display.
Pixel width of 1.
CUR OVR HCB             OKT XX7         FLW ONE SMC        RST
CUR OVR HCB             OKT XX7 Bf0     FLW ONE            RST
CUR OVR HCB             OKT XX7     Bf1 FLW ONE            RST
CUR OVR HCB             OKT XX7 Bf0 Bf1 FLW ONE            RST
CUR OVR HCB             OKT XX7         FLW ONE            RST
CUR OVR HCB             OKT XX7 Bf0     FLW ONE            RST
CUR OVR HCB             OKT XX7     Bf1 FLW ONE            RST
CUR OVR HCB             OKT XX7 Bf0 Bf1 FLW ONE            RST
CUR OVR xxx             OKT XX7 xxx xxx     ONE            RST  last pixel out of image memory registers
CUR OVR xxx             OKT XX7 xxx xxx     ONE            RST
xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx xxx  last pixel displayed by D-A converter

Note: SMC is two pixel periods earlier than in the Model 10.
```

9.N HCM Refreshing of Image Memory

The HCM can be used to generate refresh cycles during horizontal blanking, ensuring that image data is not lost. Typically, neither the PC nor the TMS320C25 access the image memory during horizontal blanking and the HCM can be programmed to generate refresh cycles during of horizontal blanking. If either processor accesses the image memory during horizontal blanking the HCM cannot generate refresh cycles at the same time. The HCM can be programmed to refresh the image memory if the HCM is not stopped during horizontal blanking or horizontal sync, and if the duration of horizontal blanking or sync is at least 6 pixel clock cycles.

The condition that the HCM not be stopped during horizontal blanking or horizontal sync constrains the use of HCM refreshing to when the Model 12 is operating in Master Sync Mode, or is operating in Genlock Mode using the on-board pixel clock generator module (referred to as Genlock Mode 1 in the **RS-170 Video Timing Generation** chapter). The HCM cannot be used to generate refresh when genlocked using an external pixel clock, because the HCM is stopped during horizontal sync.

9.O Master Mode Horizontal Video Sync Generation

In Master Mode, the HCM is used to generate horizontal video timing signals. These signals are logically combined with vertical video timing signals to form a composite sync signal. The vertical timing signals are generated by the TMS320C25 using the Vertical Control Register (VCR).

Horizontal Load (*HCMC*) loads the HCM counter. This bit **must** be 1 at the first location in the sequence. The length of the line, in pixel clocks, is determined by HCMC high.

Horizontal Composite Sync (*HCS*), is used during video display to generate a horizontal sync pulse, indicating the end of the line, which can be used to synchronize a camera or monitor. The leading (falling) edge of this signal is also used to interrupt the TMS320C25.

Horizontal Composite Blanking (*HACT*) is used to enable digitize, display, and refresh operations.

Horizontal Composite Sync Equalization Pulse Interval (*HEPI*) is intended for generation of equalization pulses. These pulses are needed when interlaced video is being digitized or displayed. They occur at the beginning of the line (when HCS occurs) and at the midpoint of the line. HEPI is gated with the VEPI signal from the VCR. HEPI is also used to interrupt the TMS320C25 processor in the middle of the line.

The *Horizontal Composite Sync Vertical Serration Pulse Interval* (*HSPI*) generates a serration pulse. This pulse is gated with the VSPI signal in the VCR. Serration pulses are used with interlaced video, and to generate a vertical sync on the COMP OUT signal.

The composite sync pulse train is composed of the HCS pulse, the HEPI pulse, and the HSPI pulses. Each pulse is logically ORed with signals from the Vertical Control Register to form the pulse train.

When the Model 12 is generating video timing, a pulse train must be generated to interrupt the TMS320C25 on either a line or half line basis. The interrupt signal is composed of the HEPI and the HCS pulse, which are logically ORed with the HLS signal from the Vertical Control Register. When HLS is low, the HEPI signal is used, causing interrupts twice per line. When HLS is high, HCS is used, causing interrupts once per line. The leading (falling) edge of the signal is used, so that the TMS320C25 has time to load image memory address counters during the horizontal blanking, as required.

Table 9-4 lists the HCM instructions to generate the correct timing, and their corresponding address in the HCM.

Address	Byte	Function
0	0x01	Cursor High, all others active
32	0x03	Equalization pulse inactive
64	0x83	H Sync inactive
84	0x82	Cursor active
88	0x83	Cursor inactive
118	0x87	Display video
391	0xC7	Serration pulse inactive
455	0x85	Serration, Equalization active
487	0x87	Equalization inactive
846	0xC7	Serration inactive
891	0xC3	Blank video

TABLE 9-4. RS-170 Timing: HCM Bits

9.P Genlock Mode Horizontal Video Sync Generation

The HCM functions differently in genlock mode than in master mode. The HCM is not generating timing signals but is used to filter horizontal sync and to blank video.

The HCM is used to filter horizontal sync signals to prevent data loss in the image memory should a sync signal occur during HCM cycles to the image memory. It does this by providing "qualifier" signals that are logically ANDed with horizontal sync. Two qualifiers are provided, one for the leading edge and one for the trailing edge of sync .

A third signal is provided for the case when *no* sync occurs after a certain time. This is designated the "overrun" qualifier and causes a HCM load and an interrupt to the TMS320C25. The overrun qualifier prevents the HCM counter from counting to its limit and then "wrapping around," or incrementing from the digitize portion of the HCM to the display portion of the HCM which may cause data loss in the image memory.

9.P.1 Qualifiers

1. **Leading Edge Qualifier.** The *HQUL* signal qualifies the leading edge of composite sync. When both HQUL and composite sync are low, a load is generated to the HCM (if HCTS in T1 is high), and an interrupt is requested from the TMS320C25. HQUL should be programmed to go low at or near the leading edge of horizontal sync, and programmed to go high 10-20 pixel clocks later.

   When HQUL and composite sync are low, and HLS is high, an interrupt will be requested on TMS320C25 level 0. HLS is an output of the Vertical Control Register. During genlock mode, HLS can be used to indicate when half line interrupts will occur. When HLS is low, qualifiers are ignored, and all sync signals will cause a HCM load and interrupt requests.

2. **Trailing Edge Qualifier.** The HSPI signal is redefined during genlock mode as a qualifier. HSPI is used to qualify when genlocked to the trailing edge of composite sync. This is most useful when digitizing from a video tape recorder. With HSPI low and composite sync high, the HCM will be loaded. An interrupt to the TMS320C25 is not requested (it is requested on the leading edge). HSPI should be programmed low at or previous to the trailing edge of composite sync. HSPI should remain low 5-10 pixel clock cycles.
3. **Overrun Qualifier.** The HEPI signal is redefined during genlock mode as the overrun qualifier. HEPI should be programmed low **after** the normal composite sync is expected. With RS-170, this would be some time after pixel clock 910. When HEPI is low and HQUL is high, HCM load is generated and the TMS320C25 is interrupted.

A simple way to defeat qualifiers is to program HQUL low, HSPI low, and HEPI high for the entire line.

Table 9-5 shows HCM instructions to generate qualifiers, and their corresponding addresses in the HCM when genlocked to RS-170 video. Figure 9-1 shows the relative timing between the qualifiers and composite sync when leading edge of composite sync is used. Figure 9-2 shows relative timing when trailing edge of composite sync is used.

Sync on Leading Edge

Address	Byte	Function
0	0xEB	Blank Video
118	0xEF	Active Video
891	0xCB	Qualify, Blank
930	0xE9	Overrun

Sync on Trailing Edge

Address	Byte	Function
0	0xEB	Blank
50	0xEF	Active Video
819	0xEB	Blank
830	0xCB	Qualify Lead Edge
860	0xEB	Lead Edge gone
900	0xBB	Qualify Trail Edge
930	0xE9	Overrun

TABLE 9-5. HCM Qualifiers

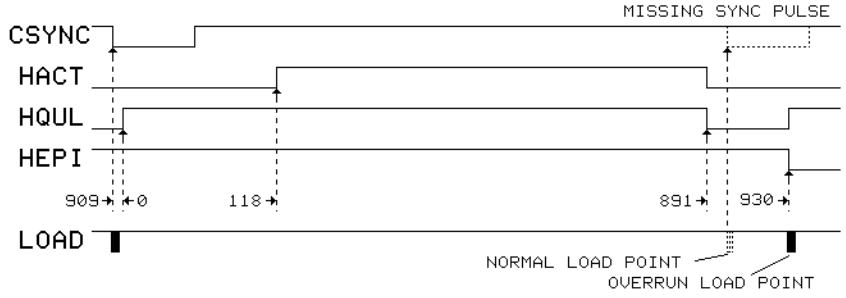

Figure 9-1. HCM Leading Edge Qualifier Signal Timing

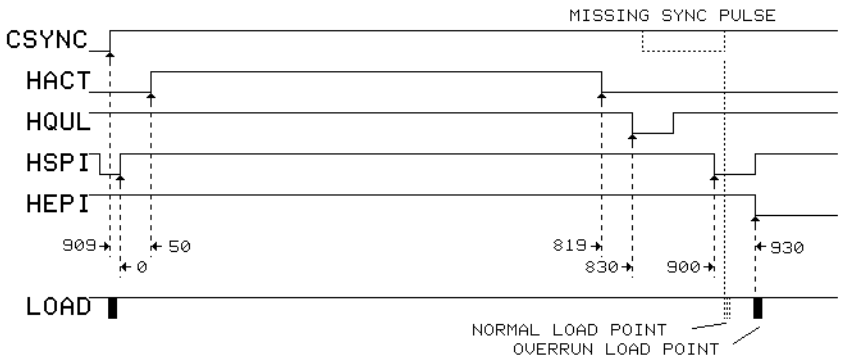

Figure 9-2. HCM Trailing Edge Qualifier Signal Timing

9.P.2 Horizontal Load in Genlock Mode

When the Model 12 is run in genlock mode and the Pixel Clock Generator Module is generating the pixel clock, the edge of composite sync that is used to load the HCM counters affects the operation of the HCM. This is due to the load being active for 1 pixel clock. The affect is to shift the portion of the line that is digitized or displayed. The shift is by the number of pixels the horizontal sync is active. For example, if the leading edge of sync is used as the load point, pixel 0 of the HCM will be 1 pixel clock cycle later. Let the first pixel with active video occur 124 pixel clocks after the leading edge of sync. The first active pixel, to the HCM, is at pixel 123. If the same format is used (first active pixel at location 123) and load is on the *trailing* edge of sync, the active video region in the HCM is shifted to the right by the number of pixel clocks from the leading edge to the trailing edge of sync. This is shown in Figure 9-3.

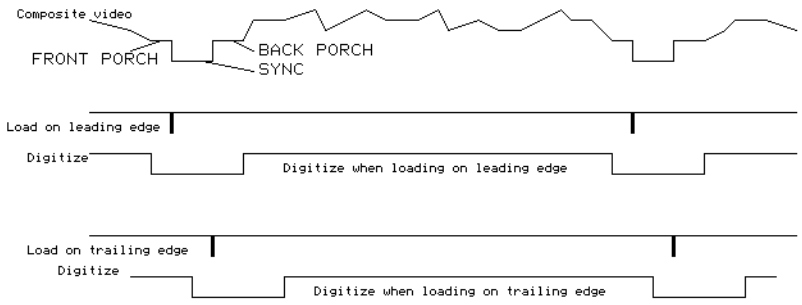

Figure 9-3. Genlock at Leading and Trailing Edge of Sync

When genlocked using an external pixel clock, the situation is similar to loading on the trailing edge, because the HCM is loaded for the duration of the sync signal. The program in the HCM for this situation should always assume pixel 0 is at the trailing edge of horizontal sync.

10. RS-170 Video Timing Generation

The Electronic Industries Association RS-170 standard provides video timing specifications for 525 lines per frame at a rate of 30 frames per second. The frame consists of two fields at a rate of 60 fields per second. Each field contains 262.5 lines. The vertical blanking time is 7.5% of the field period. During vertical blanking, special synchronization signals are generated: vertical front porch is 3 lines of equalization pulses, vertical sync is 3 lines of serration pulses, and vertical post equalization is 3 lines of equalization pulses. Vertical blanking interval consists of the 12 lines of equalization and serration followed by 9 to 12 lines of blanking.

Figure 10-1 shows the relationship between horizontal sync and composite sync at the beginning of the even field and the odd field. One vertical sync interval is offset by one half-line to interlace the two fields. At the end of the even field, one half-line of video is displayed. At the beginning of the odd field, one half-line of video is displayed.

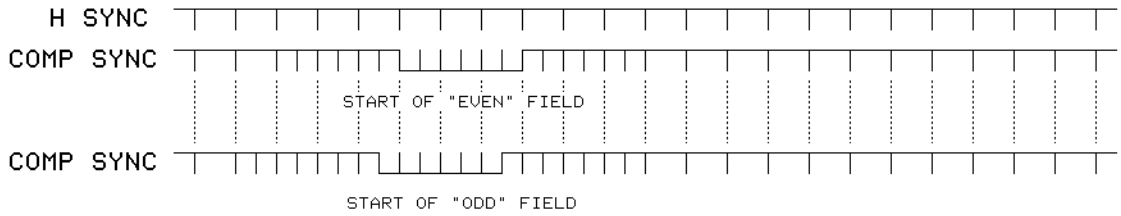

Figure 10-1. RS-170 Even and Odd Field Timing

Figure 10-1 shows the equalization and serration pulses in the vertical sync interval at the start of the even field and odd field.

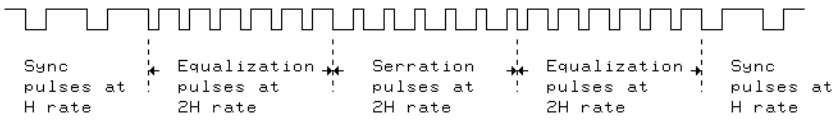

Figure 10-2. Equalization and Serration Timing

To meet the requirements of RS-170, a total horizontal line time of 63.5 μs is needed. The horizontal blanking is 17.5% of the line time. The horizontal front porch is 2.5%, and the horizontal sync is 7.5% of the line time. Equalization pulses are 3.75% and serrations are 7.5% of the line time. Serrations are used to generate vertical sync.

10.A Vertical Control Register and the HCM

When generating video timing, the TMS320C25 is interrupted on a line or half line, depending on the setting of the HLS bit. When the TMS320C25 is interrupted, the program determines the line number it is on and what to write to the VCR. VCR data is loaded into the input register. At the next interrupt, data is transferred from the input register to the output register, where it interacts with HCM signals.

On each line of video the HCM outputs a sequence of instruction words. Not every HCM signal is used on every line. During the equalization period, serrations are not needed. During active video, equalization and serrations are not needed. The VCR is used to control which waveforms are active on each line. Because the VCR is controlled by the TMS320C25, the TMS320C25 can be used to generate the sequence of timing signals required.

The signals generated by the HCM/VCR are: composite blanking, composite sync, an interrupt to the TMS320C25 on each line, a load signal for the HCM, and an arbitration signal for image memory access. The interrupt to the TMS320C25 is also used to load the vertical control output register.

10.A.1 Signal Definitions

Signal	T1 Bit
UNBLANK	bit 4
PHS1	bit 5
PHS0	bit 10
HLLE	bit 14

Signal	VCR Bit
VACT	bit 2
VSPI	bit 3
VEPI	bit 4
HLS	bit 7

Signal	HCM Bit
HEPI	bit 1
HACT	bit 2
HQUL	bit 5
HSPI	bit 6
HCS	bit 7
HUB	bit 10

! means invert
means logical OR
& means logical AND

SSCSYN is composite sync from the sync stripper
EXTHDN is horizontal drive from either the V8 Connector, the Analog Module or the sync stripper (jumper select and software select).
EXTVDN is vertical sync from either the V8 connector or the Analog Module (software select).

10.A.2 Composite Blanking

BLANKN = !VACT # !HUB # noNOno # !UNBLANK

The BLANKN signal is used to blank the RAMDAC outputs. Use of the UNBLANK signal allows software to blank the video output while digitizing. This is useful when digitizing from non RS-170 sources but displaying on an RS-170 monitor.

10.A.3 Composite Sync

!CSYN = (!PHS0 & !HCS & VEPI & VSPI)
(!PHS0 & !HEPI & !VEPI & VSPI)
(!PHS0 & !HSPI & VEPI & !VSPI)
(PHS0 & !PHS1 & !SSCSYN)
(PHS0 & PHS1 & !EXTHDN & EXTVDN)
(PHS0 & PHS1 & EXTHDN & !EXTVDN)

The CSYN signal is the composite sync signal output from the Model 12. When PHS0 is low, indicating master mode, sync is generated with signals from the HCM and the VCR, and PHS1 is used to select the pixel clock. When PHS1 is low, the pixel clock is selected with the PCLK jumper. When PHS1 is high, the pixel clock is from the V8 connector or Analog Module.

When PHS0 is high and PHS1 is low the Model 12 is genlocked to input video sync. Sync is passed directly to the COMP OUT signal on the DB25 connector thru the Analog Module. The pixel clock selected is the on-board pixel clock generator module (PCGM).

When PHS0 and PHS1 are high, the Model 12 is genlocked to horizontal and vertical inputs from either the V8 connector or the Analog Module. In this case, the composite sync out is composed of the horizontal and vertical inputs *OR*ed together.

10.A.4 TMS320C25 Interrupt Level 0

The TMS320C25 must be interrupted at the end of each horizontal line for correct operation of the Model 12. INT320 generates an interrupt to the TMS320C25 when it goes from low to high. The interrupt should always occur at the leading edge of sync. This is to give the processor sufficient time to service the interrupt before active video begins.

```
INT320 = (!PHS0 &  HLS & !HCS)
     #(!PHS0 & !HLS & !HEPI)
     #(PHS0 & !PHS1 & !SSCSYN &  HLS & !HQUL)
     #(PHS0 & !PHS1 & !SSCSYN & !HLS)
     #(PHS0 & !PHS1 & !HEPI & QUAL1)
     #(PHS0 & PHS1 & !EXTHDN)
```

In master mode (PHS0 low) the interrupt is generated by HCS or HEPI from the HCM. They are selected by the HLS bit in the Vertical Control Register. HCS generates interrupts every line, HEPI generates interrupts on half lines.

In genlock mode 1 (PHS0 = 1 and PHS1 = 0) the TMS320C25 interrupt is generated by the input composite sync, or by the HEPI bit from the HCM. To prevent the Model 12 from responding to noise on the video or composite sync input (such as from a VCR), HCM qualifying signals are used. The leading edge of horizontal sync is qualified by *AND*ing it with a qualifier bit. To select qualifiers, the HLS bit from the VCR is used. When HLS is high, the QUAL1 signal is used to qualify sync. When HLS is low, all sync signals are qualified.

The HEPI bit is used as the overrun qualifier. This loads the HCM and interrupts the TMS320C25 when no sync pulse is detected. This signal should go low some time after the interrupt is expected. Note that the composite sync signal may be polled with the BIOZ TMS320C25 instruction, to verify sync.

When genlocked to input signals to the V8 or DB25 connectors (PHS0 = 1, PHS1 = 1), it is assumed that the signals are reliable and they are not qualified at all. Note that the interrupt is generated when the signal goes low. Note that for correct operation, the horizontal sync must be present during the vertical sync period.

10.A.5 Pixel Clock Generator Module Reset

In genlock mode 1, the PCGM is synchronized with the input composite sync signal.

```
!DRESET= ( PHS0 &  SSCSYN & !HCTS & !HSPI)
     #( PHS0 & !SSCSYN &  HCTS & !HQUL)
     #( PHS0 & !HEPI & HQUL)
```

DRESET is used to reset the PCGM, in genlock mode 1, when the DRESET signal goes low. The reset synchronizes the PCGM clock with input sync and the PCGM generates a load signal to the HCM. The reset may occur on the leading or trailing edge of composite sync. The edge is selected using the HLLE bit in the T1 register (bit 14). When HLLE is high, the leading edge of composite sync resets the PCGM, and when HLLE is low, the trailing edge is used. When genlocked to a video tape recorder, better results are obtained by resetting on the trailing edge. Qualifiers are used on the leading or trailing edge, whichever is selected as the reset edge. HSPI is used to qualify the low to high transition of sync (trailing edge). HQUL is used to qualify the high to low transition (leading edge). If no edge is detected, the HEPI signal will cause an HCM load.

DRESET is not used in genlock mode 2. The HCM is loaded with input horizontal sync, and the pixel clock is input from the same source as horizontal sync. In this case, it is assumed that horizontal sync and the pixel clock are synchronous.

10.A.6 HCM or Processor to Image Memory Access

!VAHCMEN = VNFL & !HCMENBL & HCMCLRN

VAHCMEN is a Model 12 signal to arbitrate image memory accesses between the processors and the HCM (when in digitize or display). When VAHCMEN is low, video is not digitized, and the video output is blanked. Either processor can access the image memory at this time.

10.B Vertical Signal Timing

The vertical signal timing diagram in Figure 10-3 shows the relationship between vertical control signals and HCM signals.

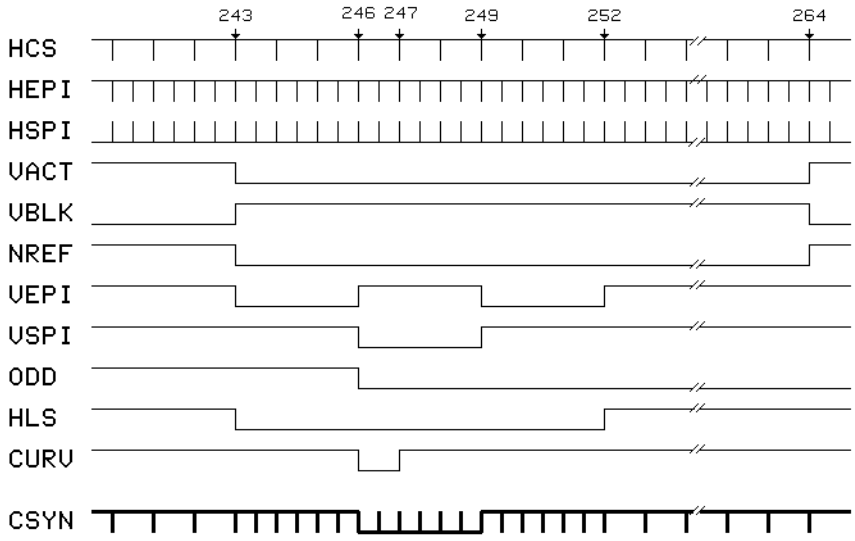

Figure 10-3. Vertical Signal Timing Diagram, Even Field

10.C Genlock

Model 12 may be genlocked to separate horizontal and vertical sync, composite sync, or composite video. Genlock operation is similar in all cases. The PCGM or an externally supplied pixel clock may be used.

When genlocked to composite sync, the input composite sync signal is buffered and output on the COMP OUT signal. The Model 12 does not need to generate any composite sync signals, simplifying operation.

The Model 12 does need to determine when vertical sync is occurring, and which field is occurring (interlaced operation). During genlock, the TMS320C25 must generate the VACT and VBLK signals for correct digitize/display operation, generate CURV for correct cursor operation, and generate NREF for memory refreshing by the PC, if needed.

10.C.1 Linear Array Camera

When working with a linear array camera (line scan camera), no vertical sync is present. Either a vertical sync must be generated (from a moving web, sheet feeder, etc.), or the TMS320C25 software must be written to start synchronization at an arbitrary point in time (perhaps on command from the AT host), and stop digitization after a predetermined number of lines have been captured (or on command from the AT host). A horizontal sync and pixel

clock are necessary for digitizing from linear array cameras.

11. Gain and Black Level Adjustment

The following procedure can be used to adjust the gain and black level of the 4MEG VIDEO Model 12 with either a line scan camera or area scan camera. The camera's video output amplitude is dependent upon the scan rate as well as the amount of light incident on the sensor. Gain and black level should be adjusted with the camera operating at the desired scan rate and with appropriate lighting.

The test target page at the back of the manual can be copied and attached to a camera stand or a wall and illuminated with the light source being used in the application. The target should fill the field of view of the camera and be in focus.

The computer chassis must be open to adjust the potentiometers on the 4MEG VIDEO Model 12. The two potentiometers to be adjusted are CLEV, which adjusts the video clamp level (black level), and GAIN, which adjusts the video gain. Turning the GAIN pot clockwise increases the gain. Turning the CLEV clockwise makes the clamp level more positive. With a non-inverted video signal this shifts the video toward low grey levels. With an inverted video signal this shifts the video toward high grey levels.

If an application note is available for the camera being used, please refer to the application note for detailed instructions.

11.A Procedure

1. Install all hardware, making sure cables are connected properly and jumpers are configured correctly.
2. Power up the PC and the camera. Point the camera at the test target and focus the lens.
3. Start 4MIP and execute the Quick Set Video file required for the camera or application (if any).
4. For slow PCs or low frequency line scan cameras, to allow the software more time to access the image memory and update the line plot faster, decrease the digitize resolution:
   - Select *Setup* from the *Main* menu.
   - Select *Digitize Video Resolution*.
   - Set the *Vert: Lines Sampled per Field* to 10.
   - Exit to the *Main* menu.
5. Select *Examine*.
6. Select *Pixel Peek, Poke & Plot*.
7. Select *Pixel Plot: Line* (*X*).
8. Place the 4MEG VIDEO Model 12 in digitize mode by holding down the Shift key and simultaneously pressing the F1 function key. A "live" line plot of one line should appear on the PC monitor.

   If the line plot is not readily visible, locate the cursor marker, at the upper left or lower left of the plot. The cursor marker is an "X", or a highlighted block, depending on the display adapter being used. When the line plot is not readily visible, the cursor marker at the top of the plot indicates that the video signal is saturated, while the cursor marker at the bottom of the plot indicates that the video signal is below the 0 level of the A-D converter.

9. Completely close the lens aperture or otherwise block all light from reaching the camera sensor.

10. If the camera provides a non-inverted video signal, adjust the CLEV pot until a horizontal line appears on the plot near the 0 grey level.

    If the camera provides an inverted video signal (such as Dalsa CA-D1 cameras) the digitized image will appear inverted. Darker areas of the image will be digitized to high grey levels and lighter areas of the image will be digitized to low grey levels. Adjust the CLEV pot until a horizontal line appears on the plot between 250 and 255. Turn CLEV counter-clockwise to "increase" the black level (higher grey levels). Turn CLEV clockwise to "decrease" the black level (lower grey levels).

11. When the black level is established, the lens aperture can be opened and the live line plot examined. The amount the lens aperture can be opened depends on the amount of light reflected off the test target and what the desired aperture may be. If the aperture is not adjustable, remove whatever was blocking the light and examine the live line plot.

    Assuming the lens has an adjustable aperture, open the aperture until the live line plot shows that a range of values is being digitized. See the figure **Pixel Line Plot of Digitized Test Target**. Note that the full range (0 to 255) may not be shown or that opening the aperture too far may cause the entire line plot to go off scale. The aperture should be adjusted so that some range of grey levels is being digitized. Adjust the focus until the high frequency peaks in the live line plot are as sharp as possible.

12. If the line plot shows that a satisfactory range of grey levels is being digitized, an image can be captured and examined by pressing the F1 function key. The image will be displayed on the video monitor, and the line plot will "freeze" on the PC monitor. Note that only 10 lines will be shown, since the resolution was set for 10 lines for ease of adjustment.

13. If opening the aperture caused the line plot to go off scale, close the aperture and adjust the clamp level until the line plot shows a horizontal line near the 128 pixel value. Gradually open the aperture until either a range of grey levels is shown, or the horizontal line goes off scale. If the line goes off scale, reduce the amount of light on the test target, close the aperture on the lens, or reduce the gain by adjusting the GAIN pot.

14. If opening the aperture shows a range of values less than what is desired, adjust the GAIN pot. Opening the aperture may affect the clamp level, requiring adjustment of CLEV. As the gain is adjusted the clamp level will also change. Adjust the gain and the clamp level until the full range of grey levels is digitized (still using the test target). With non-inverted video, keep the clamp level at 0 and adjust the gain to get the white levels at or near 255. With inverted video, keep the clamp level at 255 and adjust the gain to get the white levels at or near 0.

    Refer to the **Pixel Line Plot of Digitized Test Target**. This line plot was obtained after the gain and clamp level were adjusted to allow digitization of the full range of grey levels, using the test target at the end of the manual.

15. Once a satisfactory range of grey levels can be digitized from the test target, digitize from the target to be used in the application. If necessary, adjust gain and clamp level.

16. Once the gain and clamp level are adjusted, the resolution can be increased. Return to the *Digitize Video Resolution* menu and set the *Vert: Lines Sampled per Field* to the desired number of lines. Typing in a number such as "90000" will return with the maximum number of lines available.

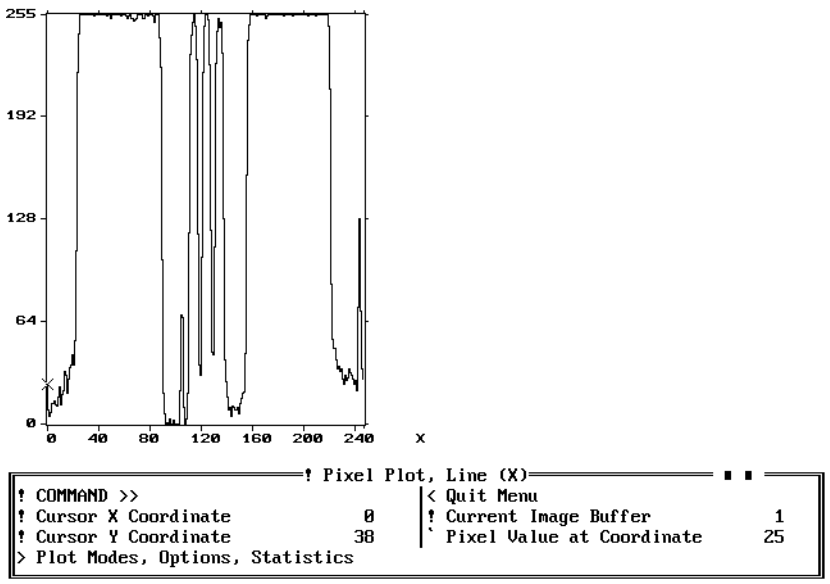

Figure 11-1. Pixel Line Plot of Digitized Test Target

12. In Case of Trouble

Two types of problems can occur with the 4MEG VIDEO Model 12: those that are detectable by software, and those that are not detectable by software.

12.A Software Detectable Errors

If error messages have occurred while attempting to execute 4MIP, note the error messages to help determine the type of problem. The source of a software detectable problem may be one or more of those listed below.

Memory Address	Two devices have the same memory address.
I/O Address	Two devices have the same I/O addresses.
Interrupt Line	Two devices are driving the same IRQ line.
Bus Timing	The bus is running faster than 8 MHz.
Pixel Clock	No pixel clock is being supplied to the card.
Defective Board	Board damaged in shipment.
No Board	The 4MEG VIDEO is not installed in the PC.

It is easy to install two devices with the same memory address, I/O address, or interrupt. It is not possible for software to determine the cause of the conflict. Take note of errors encountered and the solutions that are tried.

12.A.1 4MIP Error Messages

Prior to the display of the first menu, several tests are performed to determine and test the type of 4MEG VIDEO that is installed. If any of the critical systems fail, the software will display one of the error messages listed below, and exit. The next section describes possible causes of each message, and possible solutions to the problem.

a. Bad memory/register address? (Prog Mem error)

b. Bad memory/register address? (TMS320 RCS error)

c. HCM Mem error

d. TMS320→PC Status bits

e. PC→TMS320 Status bit

f. No PC→TMS interrupt

g. No oscillator or pixel clock? (HCM INT0 error)

h. Bad or conflicting IRQ? (No TMS→PC interrupt)

12.A.1.a Memory Address Conflicts Some of the causes of a memory address conflict and solutions are:

- LIM (Lotus, Intel, Microsoft) expansion memory, also known as "expansion memory," that occupies the same address as the 4MEG VIDEO (default 0xD0000 through 0xDFFFF) is installed and enabled. Remove, disable, or change the address of LIM memory so that is does not occupy the same address space as the 4MEG VIDEO. This can be done with the EMM.SYS (or similar) drivers, provided with DOS.
- Video adapter RAM or BIOS installed at the same address as the 4MEG VIDEO. Some 16 bit VGA or EGA adapters have memory that occupies the same addresses as the 4MEG VIDEO. If the 16 bit VGA board has the capability of sensing whether it is in an 8 bit or 16 bit slot, installing it in an 8 bit slot may free up the memory segment at 0xD0000.
- A memory expansion board may be installed at the same address as the 4MEG VIDEO. Remove, disable, or change the address of the memory expansion board.
- The PC's setup may have the memory segment for the 4MEG VIDEO disabled. Some PC's may require that "shadowing" be disabled for the 64K segment with the base address of the memory of the 4MEG VIDEO, for example, D0000.
- The PC bus does not comply with the IBM specification. Some clones only approximate the timing of the bus, which can cause incorrect data transfer from the 4MEG VIDEO to the PC, which will cause errors. Try the 4MEG VIDEO in a different machine, or try changing the bus speed.

12.A.1.b I/O Address Conflicts

- Some other hardware is installed in the machine that uses the same I/O address as the 4MEG VIDEO (default 0x280). Remove, disable, or change the address of the conflicting hardware.
- The PC bus does not comply with the IBM specification. Try the 4MEG VIDEO in a different machine, or try changing the bus speed.

12.A.1.c HCM Mem error

- The HCM memory was tested, and failed. No user solution.
- A memory address conflict with other hardware in the system. See **Memory Address Conflicts** above.
- An I/O address conflict with other hardware in the system. See **I/O Address Conflicts** above.

12.A.1.d TMS320→PC Status bits

- The status register used by the TMS320 to indicate status to the PC failed the status register test. No user solution.
- An I/O address conflict with other hardware in the system. See **I/O Address Conflicts** above.

12.A.1.e PC→TMS320 Status bit

- The status bit used by the PC to communicate with the TMS320 failed to operate correctly. No user solution.
- An I/O address conflict with other hardware in the system. See **I/O Address Conflicts** above.

12.A.1.f No PC→TMS interrupt

- The PC to TMS320 interrupt did not function. No user solution.
- An I/O address conflict with other hardware in the system. See **I/O Address Conflicts** above.

12.A.1.g No oscillator or pixel clock The HCM was initialized and started, but did not respond. There are several possible causes of this problem.

- The PCLK jumper does not have a shunt installed over any of the jumper pairs. Install a shunt over the LEFT pair, and try starting 4MIP.
- The PCLK jumper is over the LEFT pair of pins (default). Either the board is defective, the PC bus is not supplying a 14.3 MHz pixel clock, or the clock signal cannot drive the board correctly. Try a different computer.
- The PCLK jumper is over the MIDDLE pair of pins, which uses the pixel clock generator module. The pixel clock generator is not installed, not installed correctly, or is defective. Try placing the PCLK jumper over the LEFT pair.
- The PCLK jumper is over the RIGHT pair of pins, selecting an external pixel clock source. The source should be connected to the CLOCK IN signal on the DB25 connector, the Analog Module must be installed and the CK jumper must be checked to see if the 1.4 volt comparator has been selected or the potentiometer has been selected.
  - The signal is not connected.
  - The signal cannot drive the load.
  - The signal cable is defective.
  - The CK potentiometer is selected and needs adjustment.

  Try setting the PCLK jumper over the LEFT pair. If this works, then the problem is one of the four listed above.
- Bad HCM memory.
- A memory address conflict with other hardware in the system. See **Memory Address Conflicts** above.
- An I/O address conflict with other hardware in the system. See **I/O Address Conflicts** above.

12.A.1.h Bad or conflicting IRQ The 4MEG VIDEO uses IRQ level 3 as a default.

- Other devices using this level may not drive the signal correctly, causing a conflict. Try a different IRQ level, or remove the other devices in the system. Be sure to configure the software to use the new level.
- The IRQ level may have been changed (IRQ select jumper), but 4MIP may not have been configured for the new level. Start 4MIP with the following line at the DOS prompt:

  ```
  4MIP -addrs
  ```

  A menu will be displayed which allows selecting the IRQ level. See the **4MIP User's Manual** for more details.
- No shunt over the IRQ select jumper pins. Install a shunt to select IRQ 3 and retry.

12.B Other Problems

Some problems do not cause software error messages. Some problems may prevent the computer from powering up. These types of problems can be due to:

Power Supply	Insufficient power for the boards installed.
Touching Boards	One board's components are touching another board.
Defective Cable(s)	Video input or output cable has an open or short.
Video Input	Defective or incompatible video source.
No Video Output	Defective or incompatible display device or video source.
Pot Adjustment	One of the potentiometers is not set correctly.

12.B.1 Power Supply Problems

The PC power supply usually has a printed rating of power available for the four standard PC voltages. If other devices and the 4MEG VIDEO use more power than the power supply can provide, the power supply will shut down. In marginal situations, this may not happen until an operation is performed that requires additional power, such as increasing the number of pixels per line. Try removing all other boards from the system.

12.B.2 Touching Boards

If the components of one board touch those of another, damage to one or both boards can occur. Move one of the touching boards at least one slot away from the other.

12.B.3 Defective Cable

If a video input or output cable is broken or shorted, the input or output will not be connected properly.

- Try another cable.
- Test the resistance of the cable with an ohmmeter.
- Use a separate cable to connect the video source directly to a monitor or oscilloscope.

12.B.4 Video Input

If the video source is defective or incompatible, no image will be captured.

- Connect the video source directly to a monitor or oscilloscope and observe the signal.
- If the video signal is present, but is not digitized to 256 grey levels, the clamp level and/or the video gain may require adjustment. Read the "Adjustments" chapter prior to changing the potentiometer settings.

12.B.5 No Video Output

There are several reasons why no image is seen on the monitor:

- The video source may be defective, or incompatible. Note that digitizing from video sources that use a format different from what the monitor uses will probably result in a non-coherent (or blank) image on the monitor when digitizing the image.

- The monitor may be defective.
- The monitor may not be compatible with the format being displayed.
- The video output cable may be defective.
- The 4MEG VIDEO may be defective.

If no image is seen while displaying or digitizing RS-170 (or CCIR):

- With 4MIP in display mode, use *Image Test Patterns & Sequences* to generate an alignment pattern that will allow setting the contrast and brightness of the monitor. This will also verify that the 4MEG VIDEO and monitor combination are working correctly. If no image is seen:
  - Connect the GREEN output of the 4MEG VIDEO to an oscilloscope. The signal should be 1 volt peak to peak. If no signal is seen, check the video output cable.
  - Try another monitor.

  Generate a test pattern and try to digitize over the test pattern. If the test pattern has not changed:
  - Connect the video source directly to the monitor or an oscilloscope. If no signal is seen, the video source is defective, not turned on, or not plugged in.
  - Check the jumper settings on the 4MEG VIDEO. For RS-170 and CCIR, default jumper settings are sufficient for image capture and display and are given in this manual. For non-standard video sources, see the accompanying application note, or call EPIX technical support.

12.B.6 Potentiometer Adjustment

The potentiometers have been adjusted for digitizing a 1 volt peak to peak RS-170 video signal. If the video signal being digitized is not of this type, and there is a problem digitizing the signal, try to digitize from an RS-170 signal *prior* to making adjustments. A procedure for adjusting potentiometers is given in this manual.

12.C If All Else Fails

If none of the above suggestions have solved the problem, call EPIX and ask for technical support. Prior to calling, note what error messages were displayed, symptoms observed, and steps taken to solve the problem. It is helpful to call from a phone near the computer.

A board can be damaged during shipment. If damage is visible, check the shipping container for damage, and notify the freight carrier.

If the board must be returned for test or repair, call EPIX for a Return Materials Authorization (RMA) number. Be prepared to tell the technician the problem that has been encountered and what steps have been taken to attempt to correct it. Please include a written description of symptoms and error messages with the packing list of the material returned.

13. Index

14. LIMITED WARRANTY

EPIX, Inc. warrants the 4MEG VIDEO Model 12 to be in good working order for a period of one year from the date of purchase from EPIX or an EPIX distributor. Should this product fail to be in good working order at any time during this one year warranty period, EPIX will, at its option, repair or replace this product at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of EPIX.

This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse, or non-EPIX modification of the product.

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4MEG VIDEO Model 12 User's Manual

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